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STARPOWER ID- IPM Application Note



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Chapter 1 Starpower IPM Product Outlines

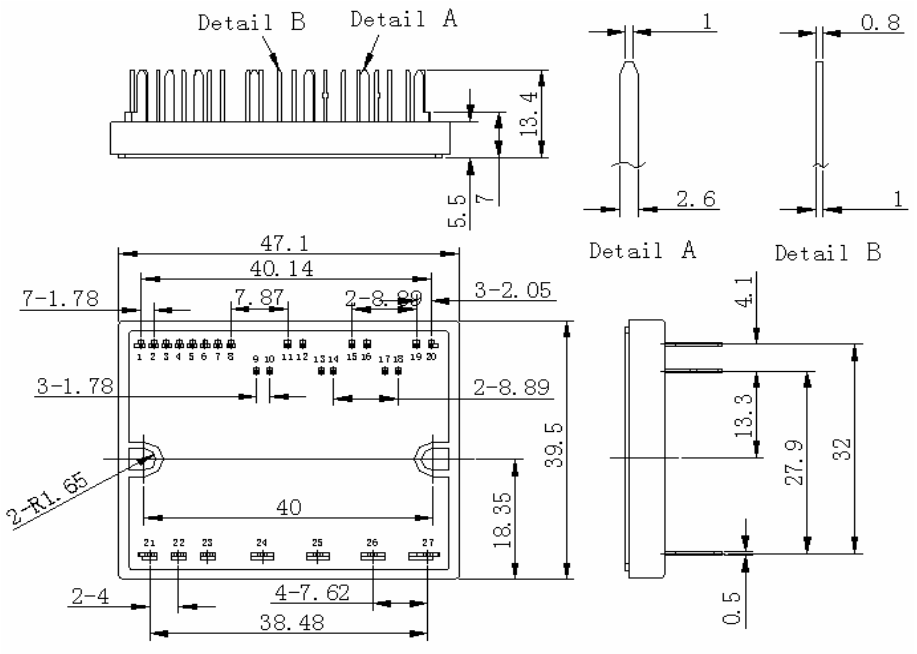
1.1 Introductions

Inverter technology brings obviously advantages like: energy efficient and quiet-running compare to the conventional motor drives technology. With the advantages of compactness, built-in control, and lower overall-cost modules requirements are increasing for low-power motor control applications. Starpower's ID series IPM is provided with compact, high-functionality, and high efficiency to meet these needs.

ID series IPM is an attractive choice which alternative to conventional discrete solution for low-power motor drives, specifically for appliances such as air conditioning, washing machines. ID series IPM combines optimized driver and protection circuit which matched to the IGBT's switching characteristics. ID series IPM is also provided with highly effective short-circuit detection and protection functions through the use of real time current sensing technique together with under-voltage protection function to prevent over heat condition when driving voltage is not working normally.

This application note shows the details of ID series IPM. The designer could easily understand and learn how

1.2.1 Drawing



TERMINAL CODE

1 VCC	15 VB(V)
2 COM	16 VS(U)
3 IN(UL)	17 IN(...)
4 IN(VL)	18 VCC
5 IN(WL)	19 VB(W)
6 VFO	20 VS(W)
7 CFOD	21 NU
8 CSC	22 NV
9 IN(UH)	23 NW
10 VCC	24 U
11 VB(U)	25 V
12 VS(U)	26 W
13 IN(VH)	27 P
14 VCC	

Figure 1-2. Package Outlines

1.2.2 Ordering Information

ID 20 F T 06 A1 S

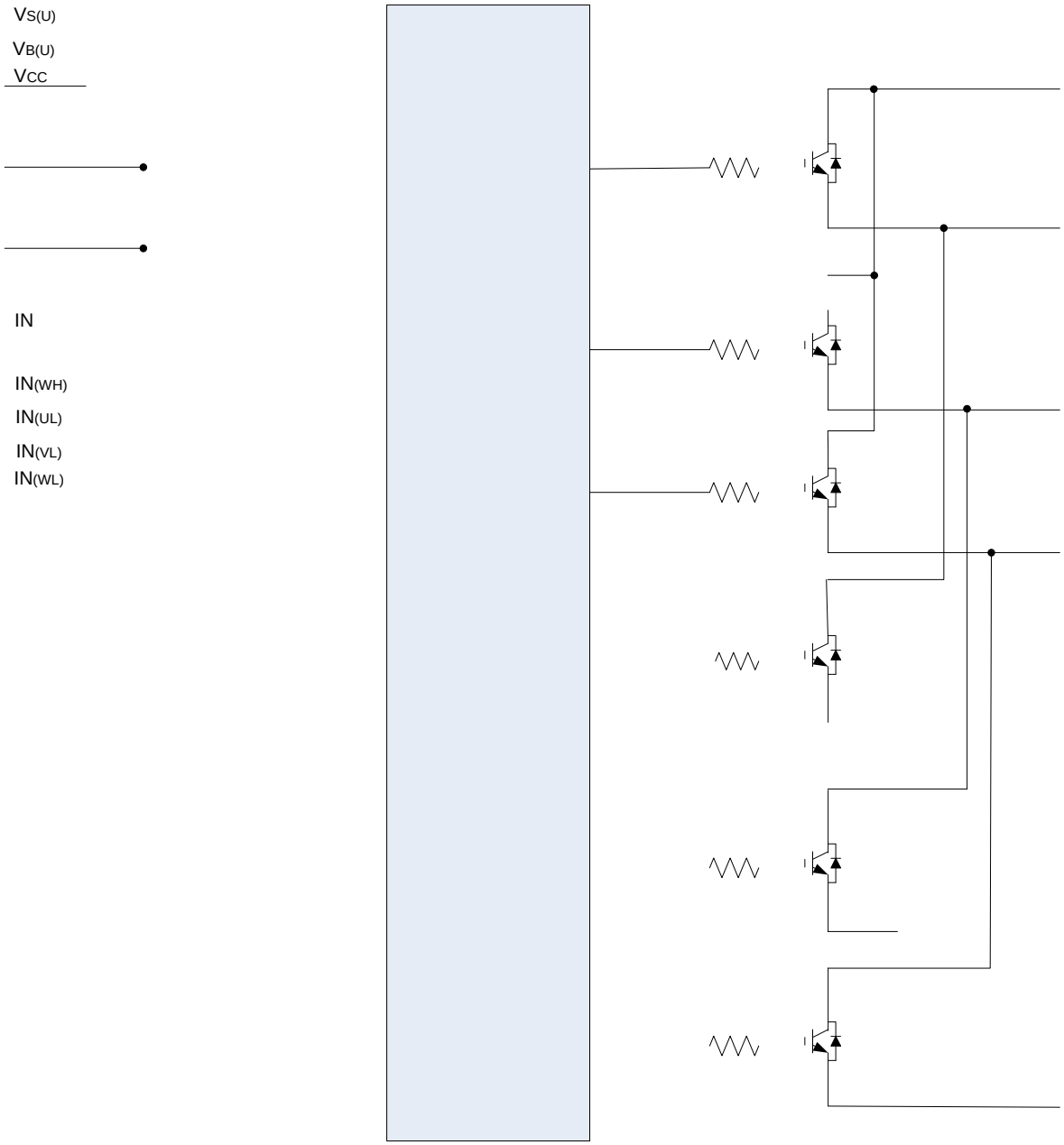
(1) (2) (3) (4) (5) (6) (7)

(1) Device: Intelligent Power Module
(2) Current Rating: 20=20A
(3) Circuit Configuration: F=Three Phase, P=Seven Pack
(4) Chip Characteristics: L=NPT Low Loss, T=Trench Low Loss
(5) Voltage Rating: 06=600V, 12=1200V
(6) Package Style
(7) Options

1.2.3 Starpower ID-IPM Series

Table 1-1. Starpower ID-IPM Series and General Applications

Part Number	Ratings	Motor Ratings(*)	PWM Frequency(Typ.)	Remark
ID10FT06A1S	600V/10A	0.5 KW/220Vac	15kHz	


VS(U)
VB(U)
VCC
IN
IN(WH)
IN(UL)
IN(VL)
IN(WL)



1.4.2 Features and Functions

Features

- UL Certified (UL 1557).
- Low power dissipation and excellent thermal package design.
- Low temperature coefficient effect both for driver and IGBT.
- Divided negative dc-link terminals for inverter current sharing application.
- Matched propagation delay for all channels.
- Lead-Free packaging and RoHS compatible.
- Provided a fault signal (V_{FO} pin) and shut-off internal IGBT when OC/SC and under-voltage event occur.

Chapter 2 Electrical Characteristics

2.1 Description of the Input and Output Pins

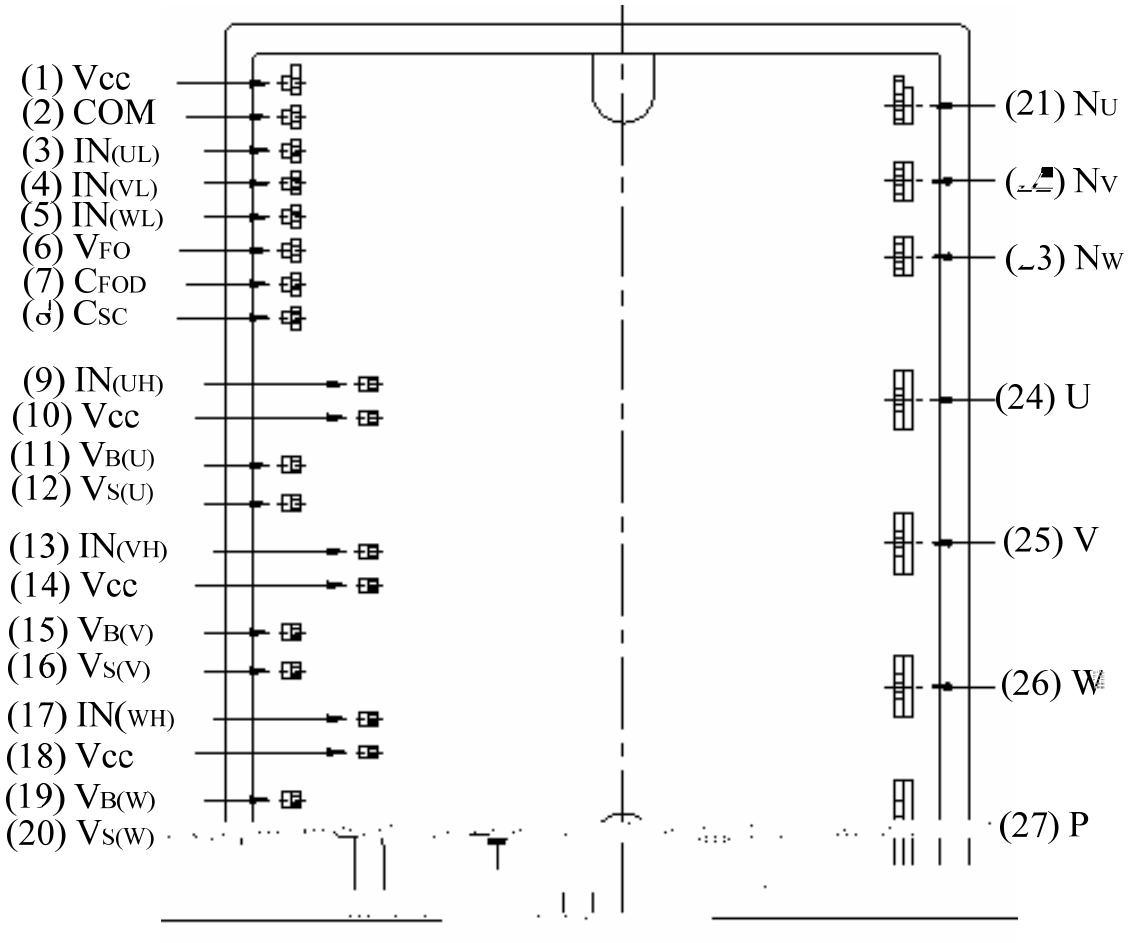


Figure 2-1. Pin Definition of ID IPM (ID20FT06A1S)



2.1.2 Pin Descrition

Supply source of the ID- IPM

Pin symbol V_{CC}

- V_{CC} is internal connected together.
- It is necessary to mount (as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.
- To prevent damage the internal driver IC. So, it is necessary to keep the operation supply voltage below the maximum specified values.

Grounding port

Pin symbol COM

- This is the driver ground for the internal driver IC.
- Main loop current of the power circuit loop should not be allowed to flow through these terminals to avoid noise influences.

Short-circuit trip voltage sensing port

Pin symbol C_{SC}

- The designer need to insert the current sensing resistor between this terminal and GND to detect OC/SC situations.
- The port may recognize the noise as the real input, so the designer need to add a suitable RC filter to reduce the noise level but don't delay the actual signal.

Fault pulse output time setting port

Pin symbol C_{FOD}

- This port is used for setting the fault pulse output time.
- In order to set the fault pulse output time, the designer may need to add an external capacitor between this port and ground (reference).

External RC network input used to define FAULT CLEAR delay, TFO, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-collector high-impedance.

Fault output port

Pin symbol V_{FO}

- This terminal will be pulled down to low level in case abnormal condition SC/OC and under-voltage lockout protection is active.

- Active logic corresponding to the state of the IGBT.
- These pins are input port which is used to detect the controlling pattern to active the IGBT for switching.
- To put RC filter in front of the input port is recommended.
- In order to eliminate the noise when the signal level is changing its state, the trace from controller to the port is recommended as short as possible.

High-side drive supply port / High-side drive supply reference port

Pin symbol $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

- The bootstrap circuit scheme is needed for driving high side IGBTs by using single supply source.
- B(x)-S(x) means the input voltage terminal for high-side IGBTs.
- It is necessary to mount(as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.

Inverter positive power supply port

Pin symbol P

- DC-Link positive terminal connected to the collectors of the high-side IGBTs internally.
- Effectively to add a good frequency characteristic capacitor to reduce the voltage spike result in persist inductance of the trace or wiring. And the smoothing capacitor is recommended to put as close to the P and N.

Inverter GND port

Pin symbol N_U,N_V,N_W

- DC-Link negative terminal connected to the emitters of the low-side IGBTs internally.
- N_U

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$IN_{(UH\ VH\ WH)}$, $IN_{(UL\ VL\ WL)}$ ON threshold voltage	$V_{IN\ (on)}$		2.5	--	--	V
$IN_{(UH\ VH\ WH)}$,$IN_{(UL\ VL\ WL)}$ OFF threshold voltage	$V_{IN(off)}$		--	--	0.8	V
$IN_{(UH\ VH\ WH)}$ input bias current	$I_{IN(UH\ VH\ WH)(HI)}$	$V_{IN(UH\ VH\ WH)}$ = 5V	-	-	200	A
	$I_{IN(UH\ VH\ WH)\ (LO)}$	$V_{IN(UH\ VH\ WH)}$ = 0V	-1	-	-	
$IN_{(UL\ VL\ WL)}$ input bias current	$I_{IN(UL\ VL\ WL)\ (HI)}$	$V_{IN(UL\ VL\ WL)}$ = 5V	-	-	200	A
	$I_{IN(UL\ VL\ WL)\ (LO)}$	$V_{IN(UL\ VL\ WL)}$ = 0V	-1	-	-	
Driver IC supply voltage	V_{CC}		11.5	15.0	20.0	V
P - side floating supply voltage	$V_{B(U)S(U),\ B(V)S(V),\ B(W)S(W)}$		11.5	15.0	20.0	V
V_{CC} terminal input current	I_C		-	1.6	2.3	mA
Fault output voltage	V_{FOH}	V_{SC} =0V	4.9	-	-	V
	V_{FOL}	V_{SC}=1V	-	-	200	mV
Short circuit trip level	$V_{SC(ref)}$	V_{CC} =15V, T_j = 25	0.45	0.50	0.55	V
Fault output pulse width	t_{FOD}					

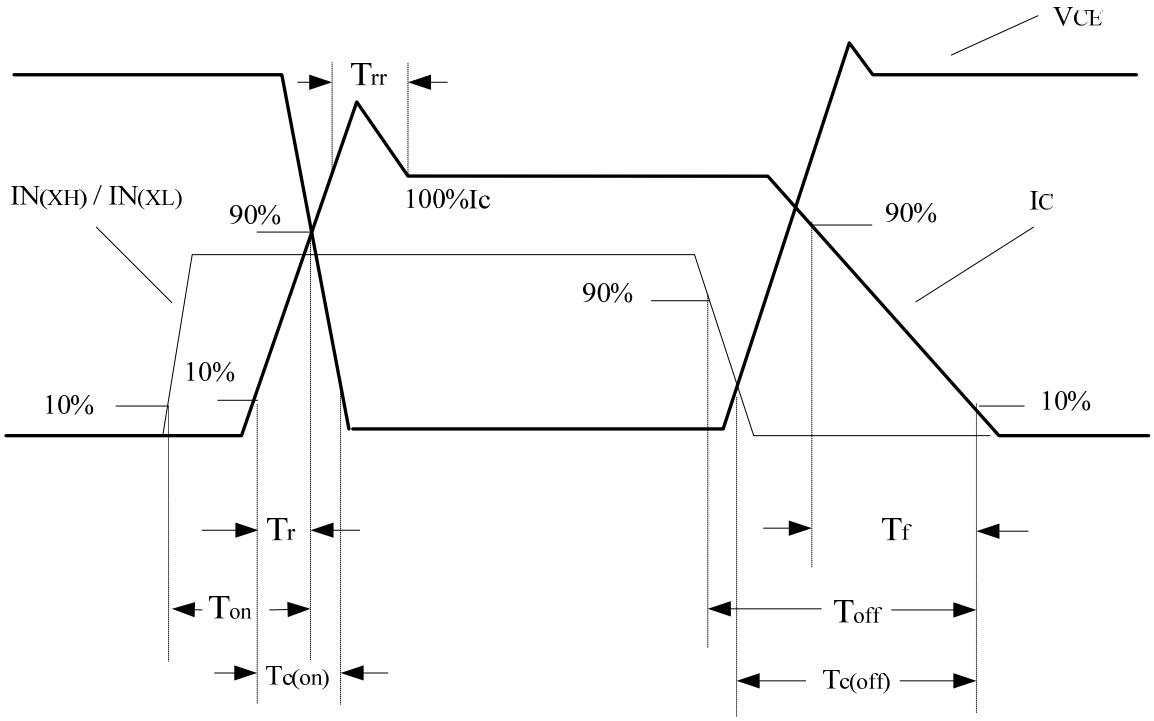
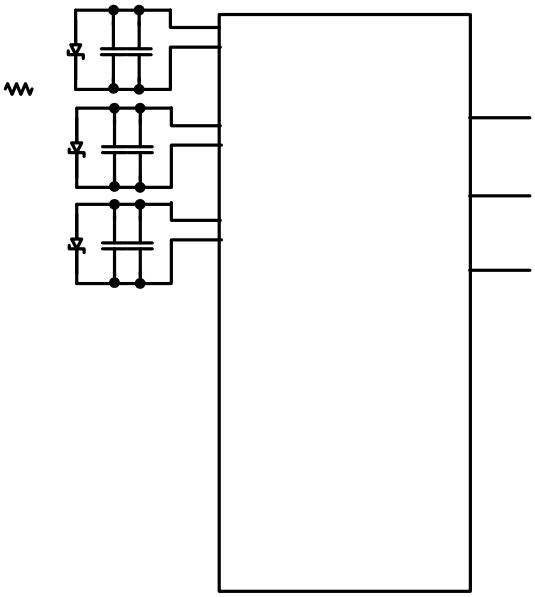


Figure 2-2. Definition of Switching Time



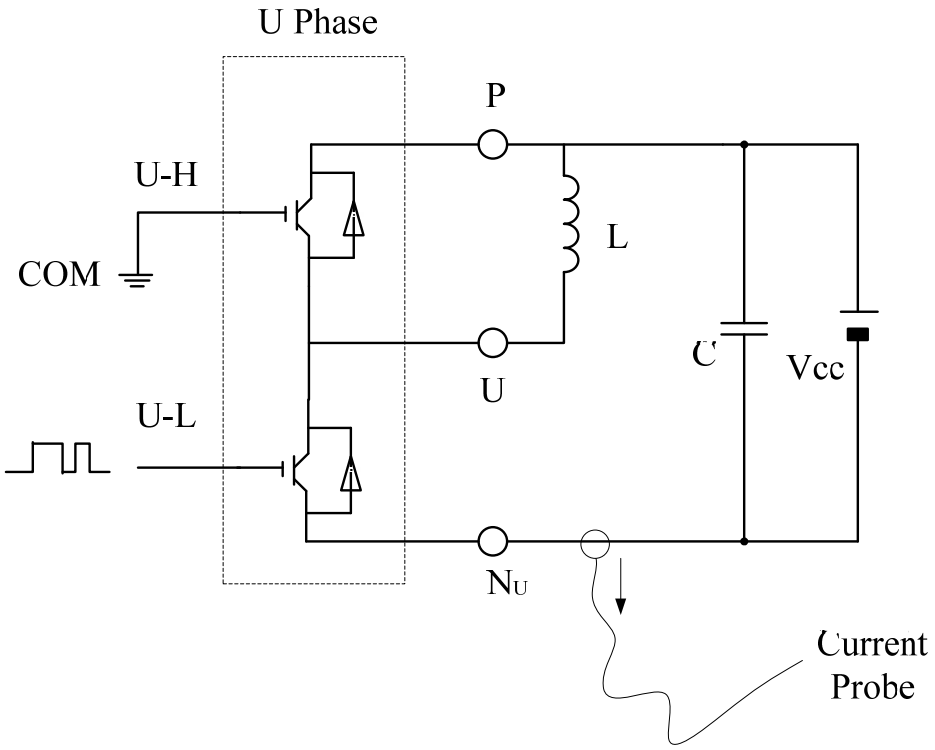
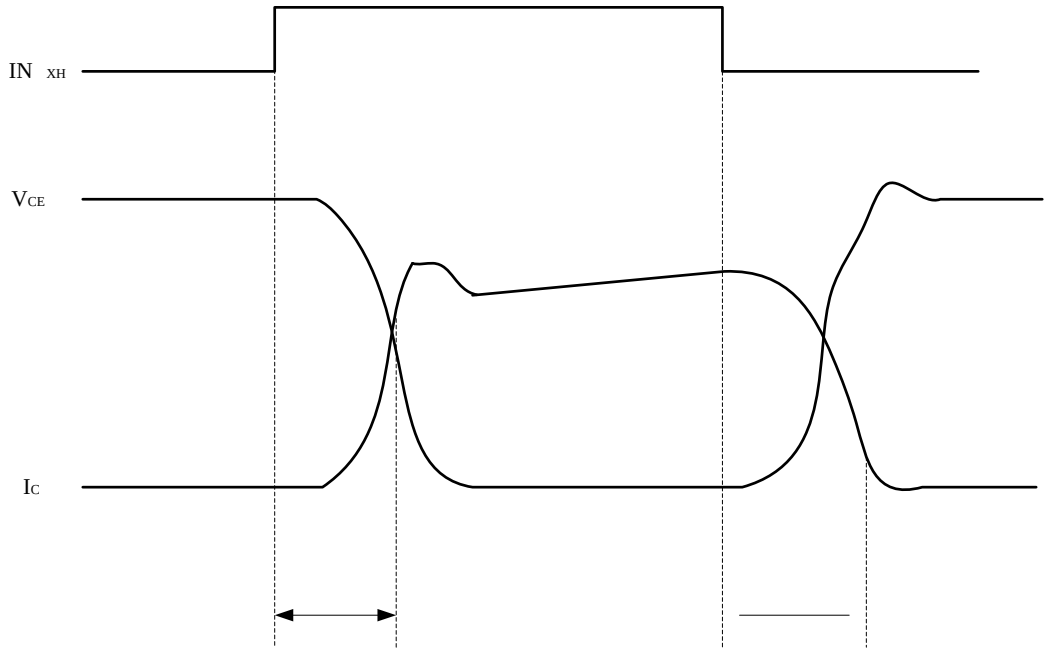


Figure 2-4. Test Circuit of Dynamic Parameter

Switching Characteristics

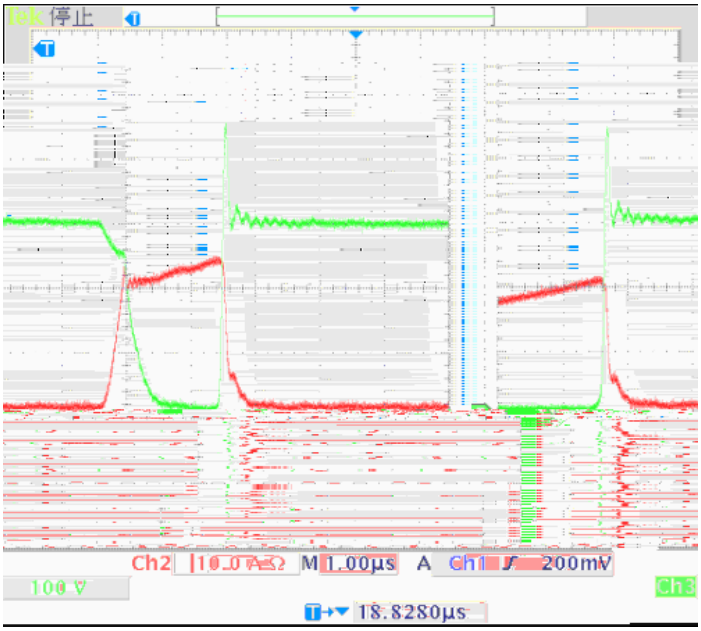


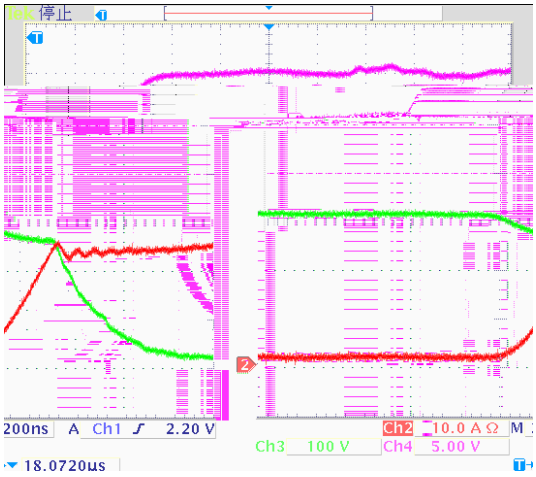
STARPOWER SEMICONDUCTOR LTD.

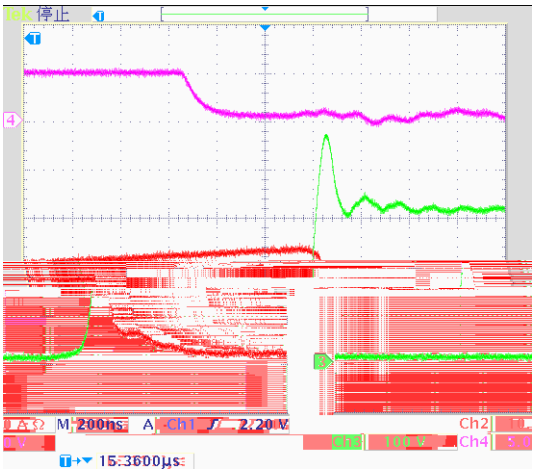
Part NO. ID20FT06A1S

Test Conditions V_{DC} = 300V, V_{CC} = 15V, I_C = 20A, Vin = 0V 5V, T_C = 25 , Inductive Load Circuit

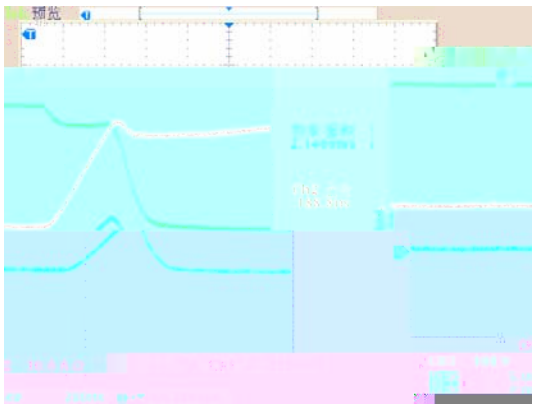
Ch2: I_C
Ch3: V_{CE}

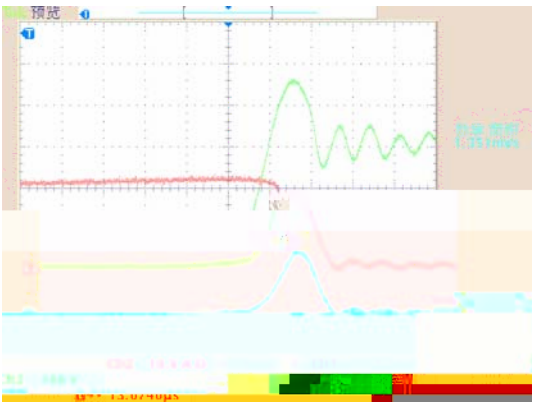






Ch2: I_C
Ch3: V_{CE}
Ch4: $IN_{(UH)}$





Ch2: I_C
Ch3: V_{CE}
M: Switching Loss

Figure 2-6. Switching Waveform of ID- IPM (Used ID20FT06A1S class) (Typ.)

Chapter 3 Packaging and Installation Guide

3.1 Package

3.1.1 Internal Structure Overview

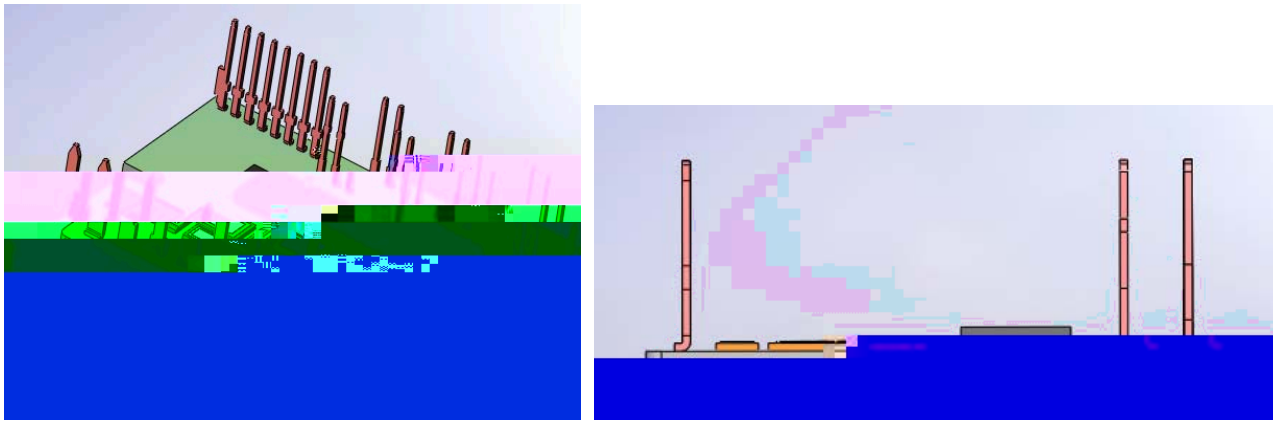


Figure 3-1. ID IPM Internal Structure

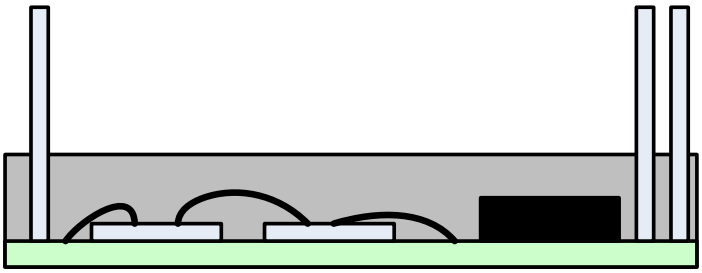


Figure 3-2. ID-IPM Package Cross Section

3.1.2 Driving and Protection Functions

Driving logic

- When the logic level of $IN_{(xH)}$ or $IN_{(xL)}$ is in high state then its corresponding IGBT will be “ON”. And when $IN_{(xH)}$ or $IN_{(xL)}$ is in low state then its corresponding IGBT will be “OFF”.
- Under-Voltage protection: if the input level of $V_{IN(xH)\ \&\ IN(xL)}$ is higher than $V_{th(on)}$ then IPM will work normally, If the input level of $V_{IN(xH)\ \&\ IN(XL)}$ is lower than $V_{th(off)}$, then IPM will shut-off its output.

Short circuit protection

- Usually the designer will use external shunt resistance to detect the injection DC-Link current to protect the load. When the current exceeds a preset SC trip level, it is judged as a short circuit state, and IPM will shut off its output immediately.
- Once the current is over the current limitation pa

Control supply circuit under voltage protection

· The protection is used to make sure the control supply

When attaching a heat-sink to an ID- IPM. Make sure not to apply excessive force to the device for assembly. Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions of indentations. Do not touch the heat-sink when IPM is operation to avoid sustaining a burn injury. Table 2-2 can provide the designer the guideline. Heat sink flatness is prescribed as seen in Figure 2-4.

Table 3-1. Mounting Torque and Heat Sink Flatness Specifications

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw M3	Recommended 0.65 N•m	0.60	0.65	0.70	N•m
Heat-sink flatness		--	-50	-	0	m

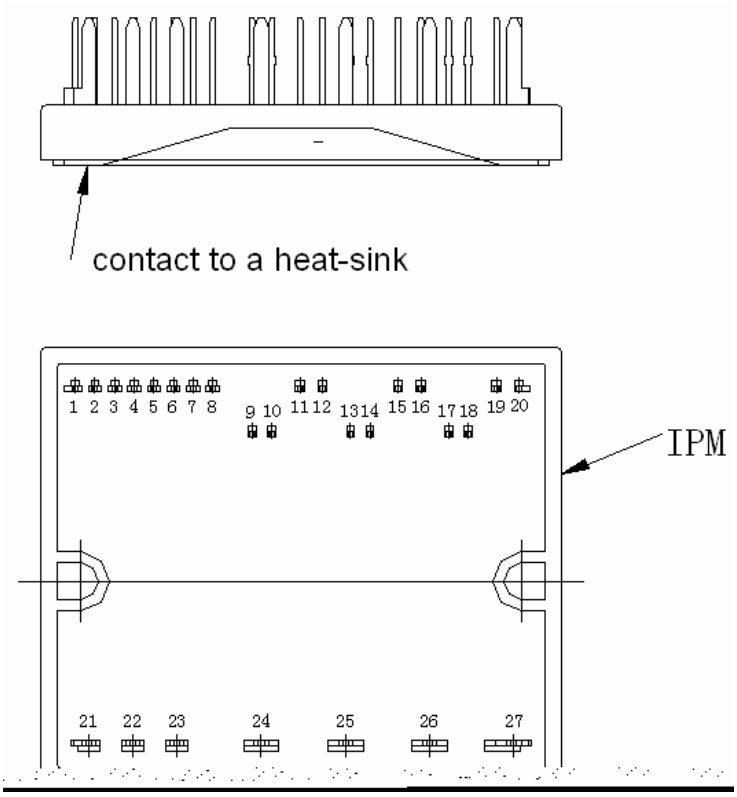


Figure 3-4. Measurement Point of Heat-sink Flatness

3.2.2 Screw Tightening Torque

Do not exceed the specified fastening torque. Over tightening the screws may cause molding compound crack and bolts with heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in table 2-2 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device. Avoid stress due to

tightening on one side only. Figure 2-5 shows the recommended fastening order for mounting screws. In the first use screwdriver temporary fastening screws, then use screwdriver permanent fastening. Note that uneven mounting can cause the ID-IPM housing and molding compound to be damaged.

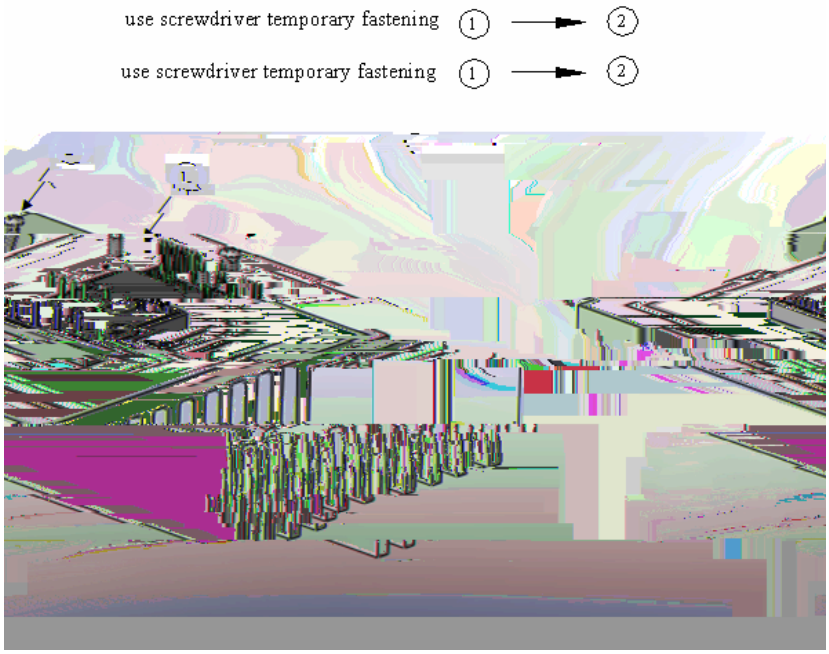


Figure 3-5. Recommended Fastening Order of Mounting Screws

The heat sink flatness (warp/concavity and convexity) on the module installation surface (refer to Figure 2-6), please follow the guidelines below in order to get effective heat-radiation when you want to enlarge the heat area.

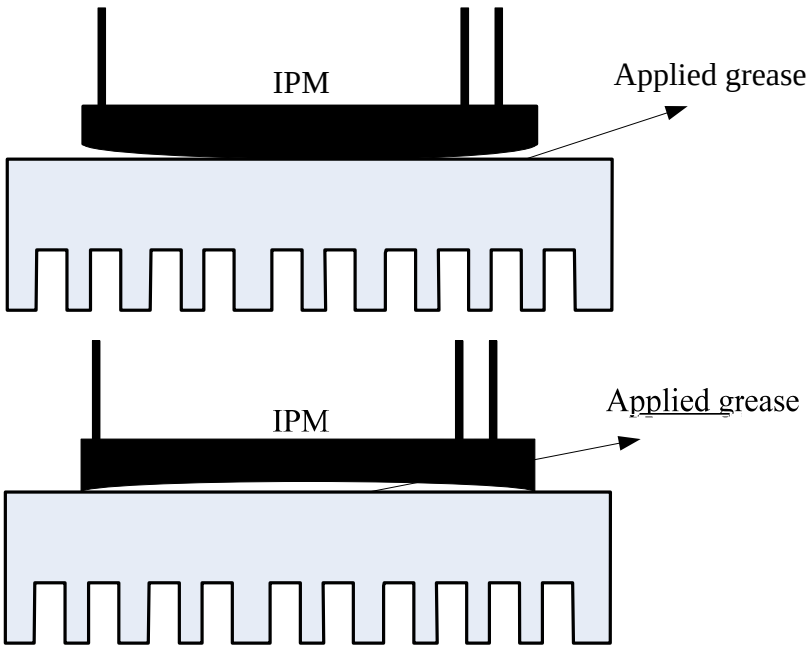


Figure 3-6. Heat Sink Flatness Specification

It will get better 100 m ~ 200 m of thermally-conductive grease over the contact surface between a module and a heat sink. It is also useful for preventing the contact surface from being corroded. Further, use a grease type of stable quality within the operating temperature range and have long endurance. Use a torque wrench to fasten up to the specified recommended torque. Exceeding the max data, torque limit might cause the modules to be damaged or to be degraded as the above-mentioned fastening with uneven stress. Foreign matter onto the contact surface between a module and a heat sink will be worse the contacting.

3.3 Handling Precaution and Storage Notices

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Be careful to handle the device and packaging material. Ensure that the device is not subjected to mechanical vibration or shock during transport. Do not toss or drop to ensure the device is O.K before on board. Wet condition is dangerous. Moisture can also adversely affect the packaging. Place the devices in the

- Be sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.
- To wear finger cots or gloves protected against static electricity if the .ktan body comes into direct contact with a device,
- When .kmidity in the working environment decreases, the .uman body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended .kmidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.
- All equipment and tools in the working area are grounded to earth is necessary.
- Take other appropriate measures, or place a conductive mat over the floor of the work area, or so that the floor surface is grounded to earth and is protected against electrostatic electricity.
- Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic taterial that allows rapid stat ic discharge when a charged device touches it directly.
- Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.
- Install antistatic mats on storage s.elf surfaces.
- For transport and temporary storage of devices, use containers that are tade of antistatic materials of materials that dissipate static electricity.
- Operators must wear antistatic clothing and condkctive shoes (or a leg or heel strap).
- Operators must wear a wrist strap grounded to earth through a resistor of about 1MΩ.
- If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a condkctive c.kcking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

Electrical Shock

- Do not touc. the device unles s you are sure that the power to the measuring instrument is off to avoid electrical measurement poses the danger of electrical shock for the device.

3.4 Marking Specification

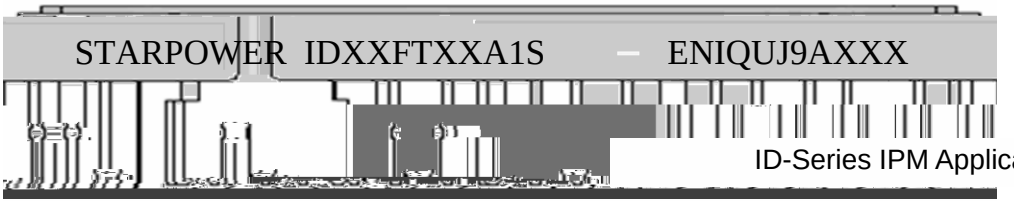


Figure 3-7. Marking Layout

1. IDXXFTXXA1S : ID series modeling ex:ID20FT06A1S sepc ID IPM 600V 20A
2. ENIQUJ9AXXX: Lot number ex:ENIQUJ9A003 ID 2009 08 3th Number

Chapter 4 Applications

4.1 System Connection Diagram

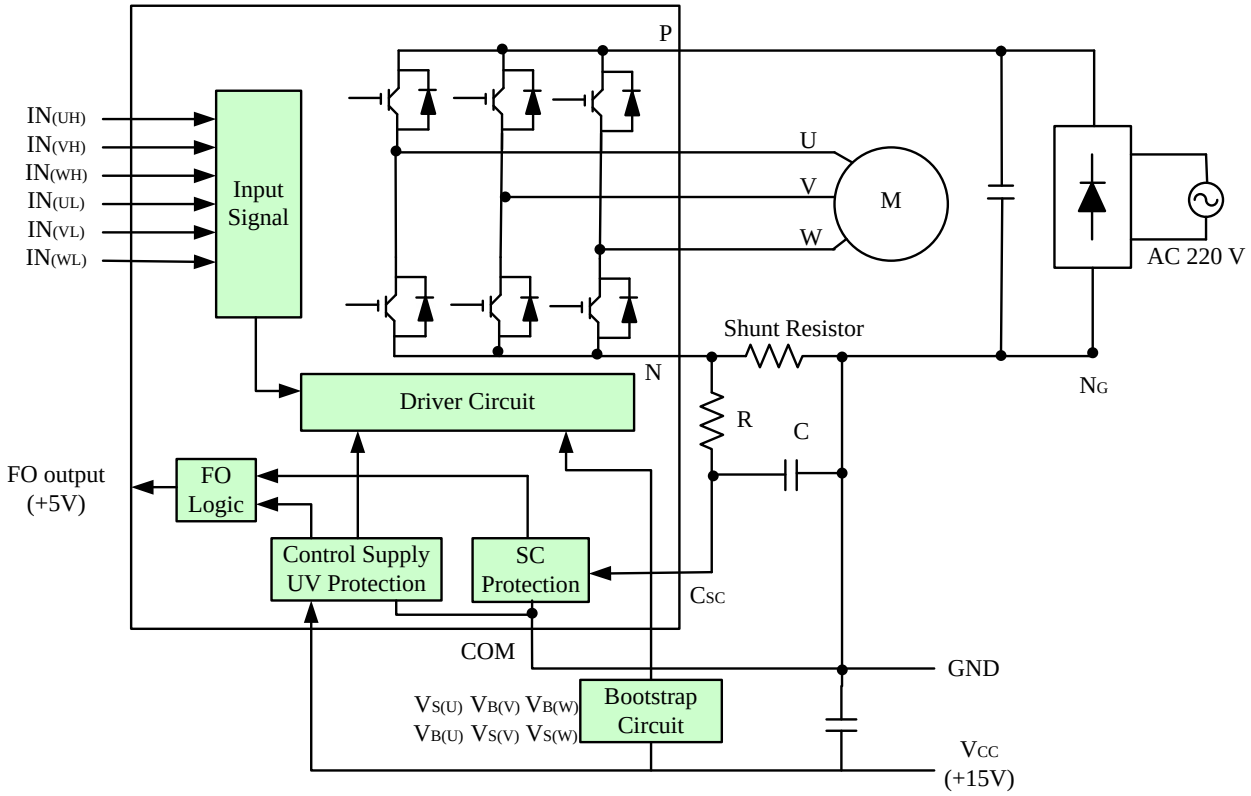


Figure 4-1. System Block Diagram of the IPM

4.2 Structure of Signal Input Terminals

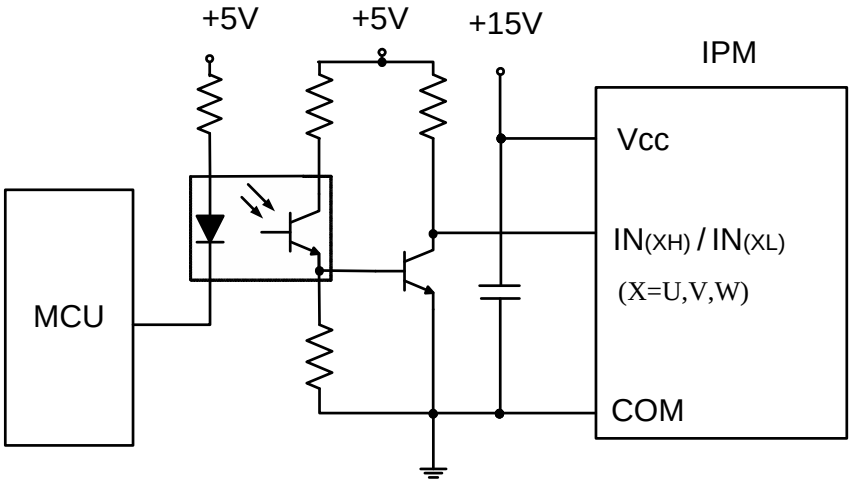


Figure 4-2. Interface Circuit Between ID-IPM and MCU

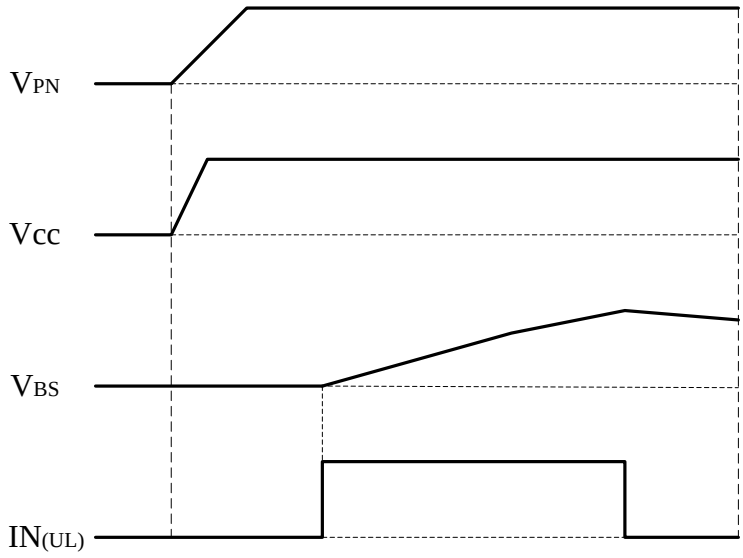


Figure 4-5. Timing Chart of Initial Bootstrap Operation Charging

The bootstrap capacitor charging and discharging timing chart is shown as Fig 4-7. We can see that the voltage V_{BS} is not a pure DC level and it has an inherently fluctuating voltage waveform because it is a floating supply due to bootstrap action.

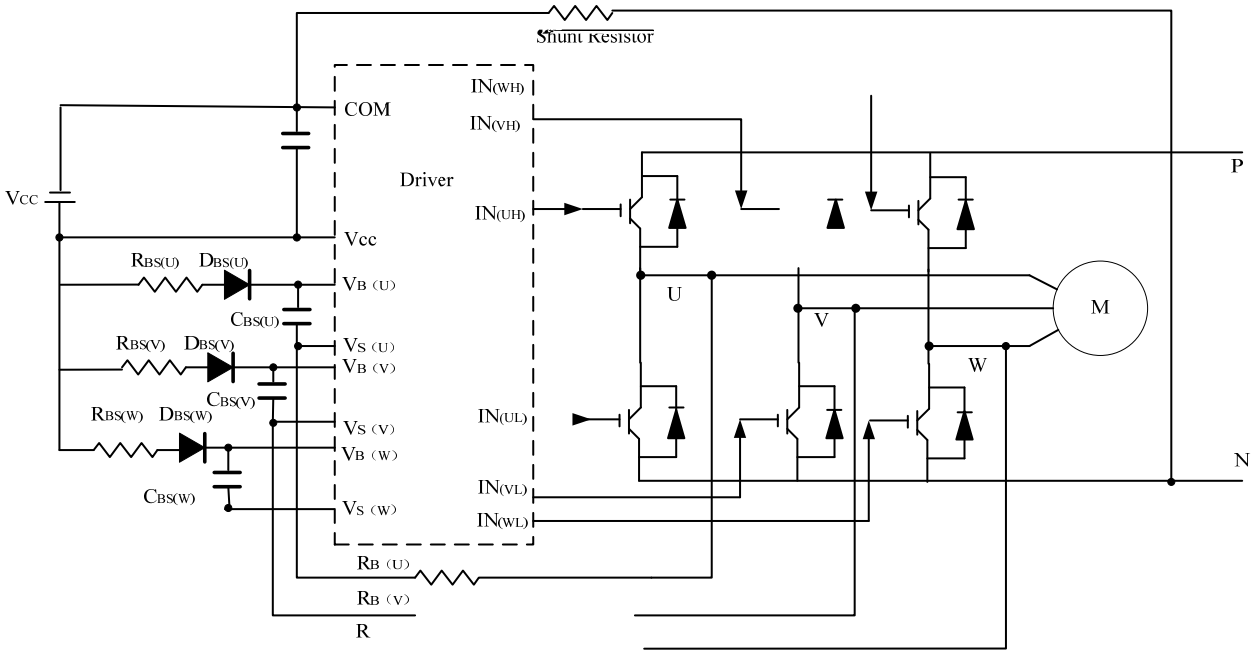


Figure 4-6. Inverter Circuit Diagram

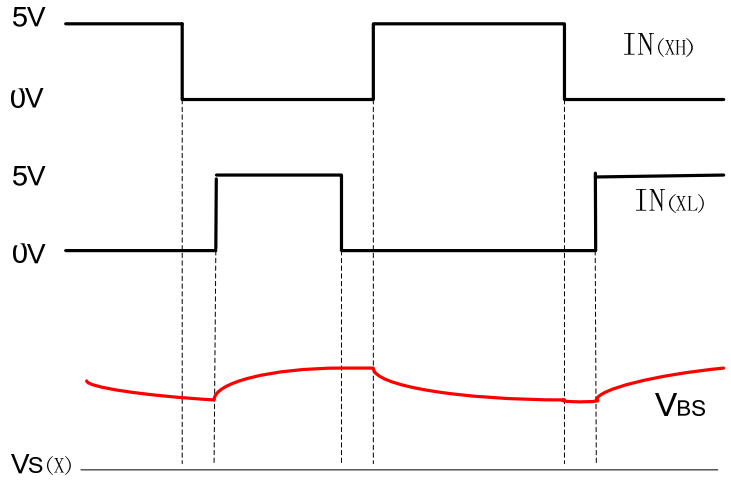


Figure 4-7. Charging and Discharging Action of the Bootstrap Capacitor Timing Chart

4.3.2 Initial Charging of a Bootstrap Capacitor

An adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time t_{charge}

Q_g = Gate charge of the high-side of the IGBT
f = Switching frequency
$I_{CBS(leak)}$ = Bootstrap capacitor leakage current
$I_{GE(leakage)}$ = Gate to emitter leakage current for the driver IC
Q_{LS} = Level shift charge required per cycle = 5nC(built in driver IC)

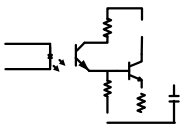
The bootstrap capacitor must be able to supply this charge Q_{BS}, and retain its full voltage. Otherwise, there will be a significant amount of ripple on the V_{BS} voltage, which could fall below the V_{BSUV} (under-voltage detection level). Hence, it is recommended that the charge in the C_{BS}

4.3.5 Bootstrap Diode Selection

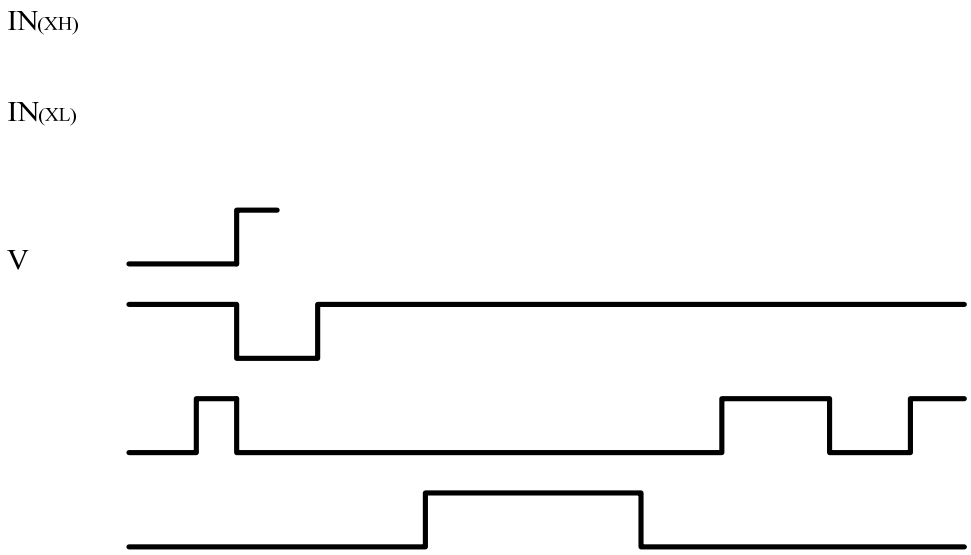
The bootstrap diode D_{BS} is used for blocking the inverter DC-link voltage when the high-side device is switched “ON. So the bootstrap diode with withstand-voltage more than 600V is recommended. It is also important that the diode should be an ultra-fast recovery device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high temperature reverse leakage current would be important if the capacitor has to store a charge for long periods of time.

4.4 Application Circuit and Recommended Parts

4.4.2 Interface Example When a Photo-Coupler is Used



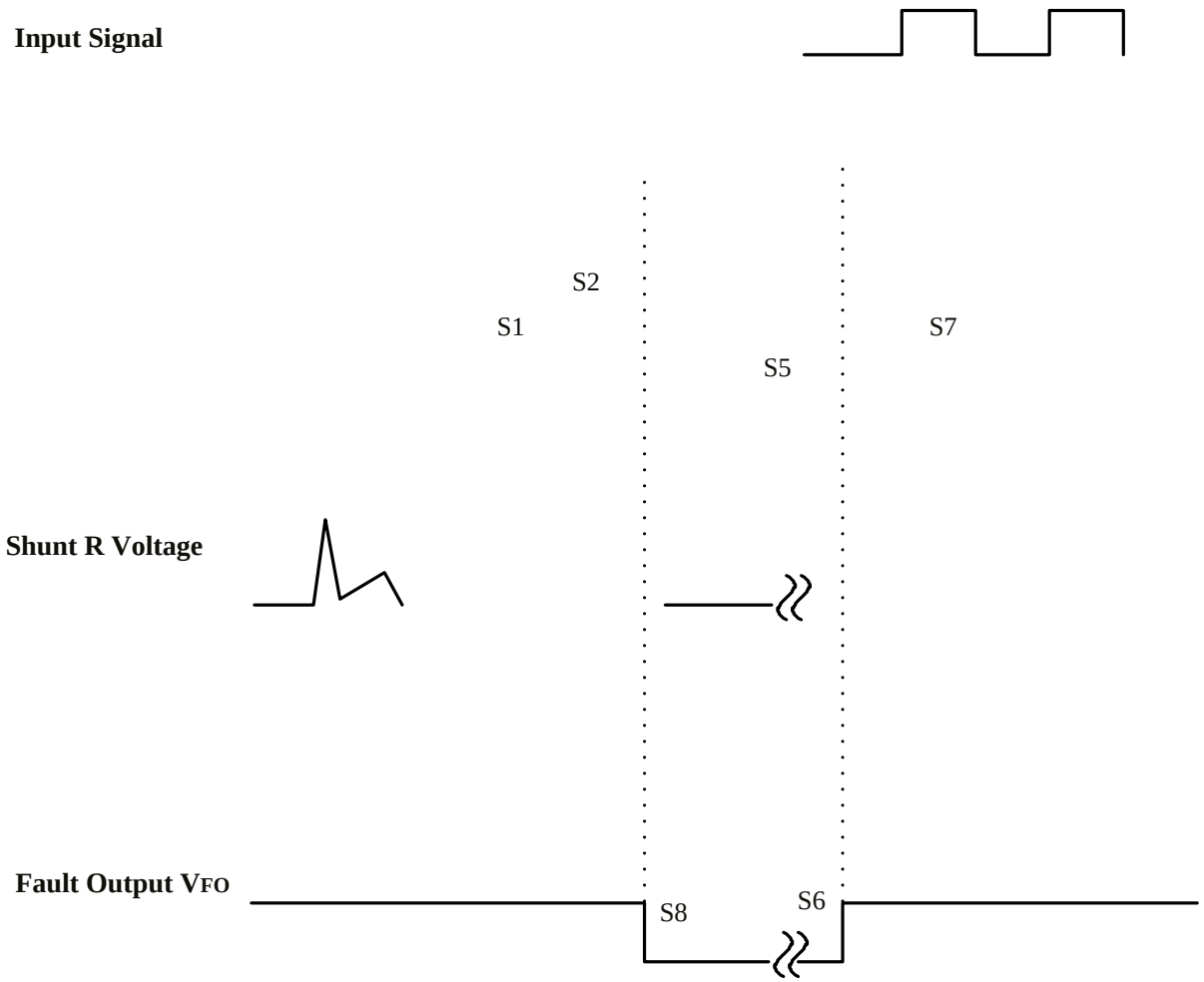
4.5 Input / Output Timing Diagram



4.6 Function and Protection Timing Charts

4.6.1 Timing Charts of Short Circuit Protection

(For the external shunt resistor and RC time constant circuit connected)





- Figure 4-14. shows the relationship between sensing resistor values and interrupted current values, based on various conditions including fluctuation range described in Table 4-6.

- In the actual design, the filter circuit would be necessary and the sensing resistor value should be evaluated.

Table 4-6. Specification for $V_{SC\ (ref)}$

Condition	Min.	Typ.	Max.	Unit
$V_{SC(ref)}$ specification at T_a=25 (Typ.)	0.45	0.50	0.55	V

Example

Sample NO. ID20FT06A1S (20A/600V)

The maximum recommended short-circuit trip current is 1.7 times the nominal IC rating of the module

Isc(max) = Ic(rating) × 1.7 = 20 × 1.7 = 34A

The minimum allowable shunt resistance is determined by requiring that the protection must operate at Ic = 34A, even if the modules short-circuit detection reference level (Vsc(ref)) is at its maximum. Referring to Table 4-6. for Vsc(ref) the minimum shunt resistance is

Rshunt(min) = Vsc(ref)max / Isc =0.55 / 34 = 16.1 mΩ

If the tolerance of the shunt resistor is 5% then the possible range is

Rmin = 16.1 mΩ, Rtyp = 17.0 mΩ, and Rmax = 17.8 mΩ

The typical short-circuit trip current is

Isc(typ) = Vsc(ref)typ / Rtyp = 0.46 / 0.017 = 27.06A

The minimum short-circuit trip current is

Isc(min) = Vsc(ref)min / Rmax = 0.37 / 0.0178 = 20.78A

Therefore, the range for short-circuit trip current is from 20.78A to 27.06A.

4.6.5 Filter Circuit Setting (RC Time Constant) for Short-Circuit Operation

Example of IPM Short-circuit Protection External Parts

The IPM have an integrated short-circuit protection function. T

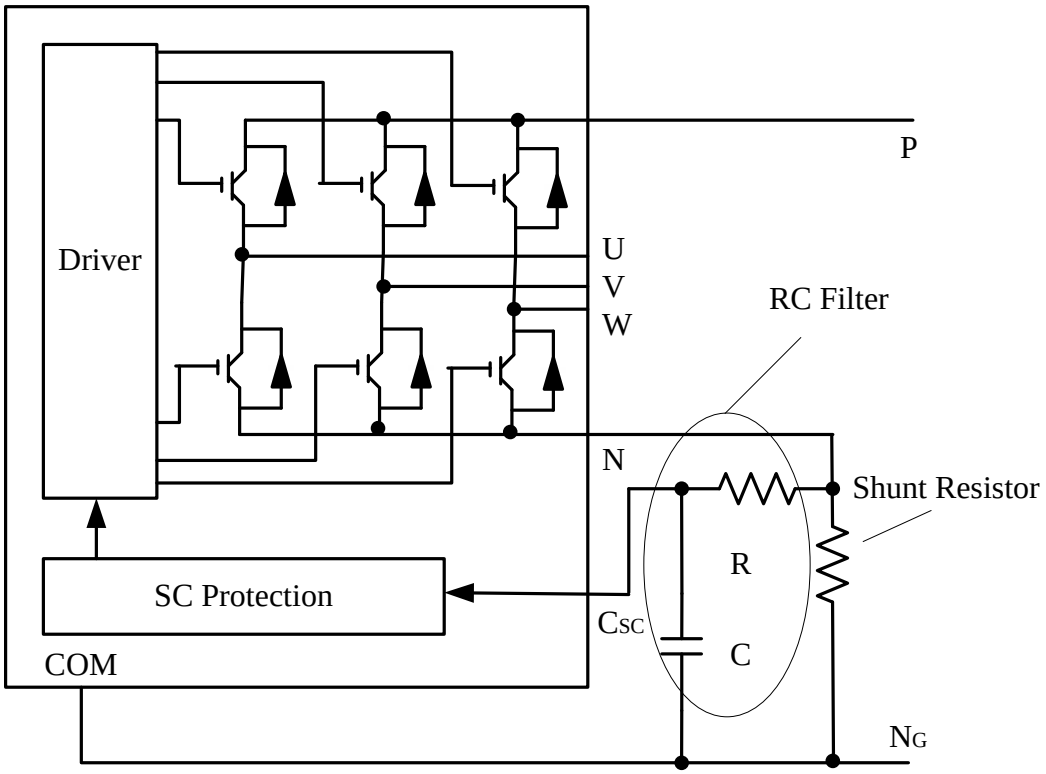


Figure 4-15. Example of External RC Filter Circuit

Figure 4-16 shows the example of external SC protection circuit. If the output current exceeds the SC trip level, all the gates of each IGBT are interrupted and the fault signal FO is outputted. The system operation should be stopped immediately when the fault output signal is pulled low.

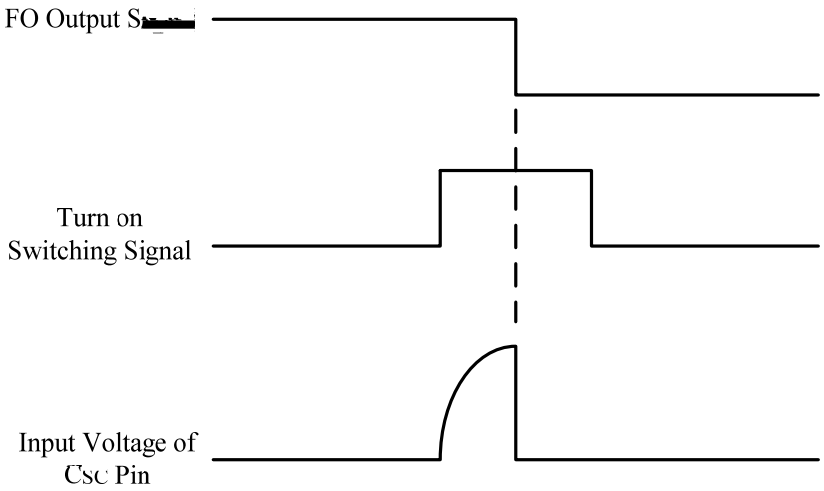


Figure 4-16. SC protection waveform

• Characteristics of RC Filter Circuit

When the RC filter circuit is connected, it can prevent the noise on the shunt resistor to make the SC protection

malfunction. The RC filter circuit immediately interrupts short-circuit currents due to its characteristics (shown in Figure4-17.) Figure 4-8 and Figure 4-9 show the recommended schemes for the different application of signal input. The RC time constant is determined depending on the applying time of noise interference and the withstand voltage capability of the IGBT.

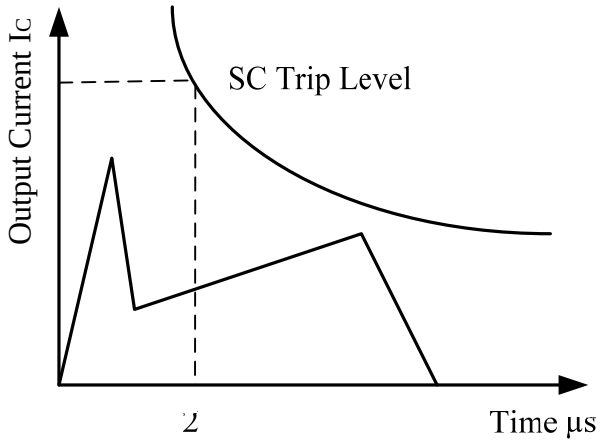


Figure 4-17. Characteristics of RC Filter Circuit

• Setting of RC Time Constant

An RC filter (R, C) should be inserted between the current sensing resistor and the IPM CIN pin as shown in Figure 4-15. The RC filter helps prevent erroneous fault detection due to di/dt noise on the shunt resistor and free-wheeling diode recovery current pulses. The RC filter also has the added advantage of producing a time

In order to prevent ID-IPM from extra surge destruction, the wiring length between the smoothing capacitor and ID-IPM P-N terminals should be as short as possible. Also, a 0.1-0.22 μF/630 V snubber capacitor should be mounted in the DC-link close to ID-IPM.

There are three positions (A, B, C) to mount a snubber capacitor as shown in the fig.4-18.

If the snubber capacitor is installed in wrong location 'A' as shown in the Figure, the snubber capacitor cannot suppress the surge voltage effectively.

In order to suppress the surge voltage maximally, the wiring connect to the P port should be as short as possible when mounting a snubber capacitor outside the shunt resistor as shown in position B. If the sunbber capacitor is installed in the position B, that will suppress surge voltage effectively. However, the charging and discharging current generated by the wiring inductance and the snubber capacity will flow though the shunt resistor, which might cause erroneous protection if this current is large enough.

In a word, the "C" position surge suppression effect is gr

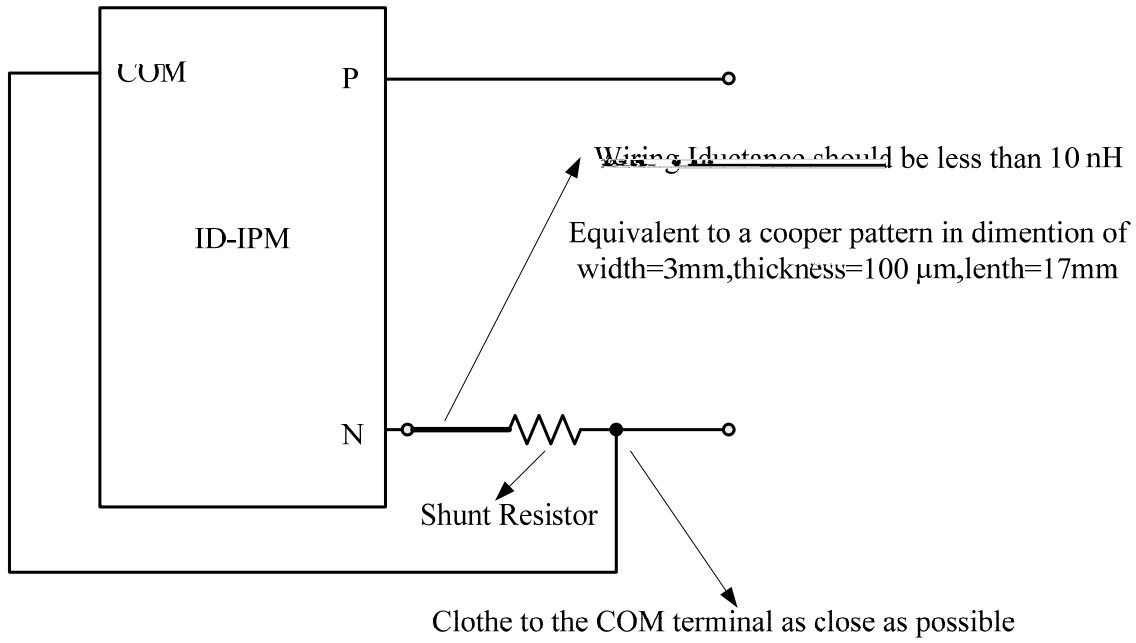


Figure 4-19. Recommend Wiring of Shunt Resistor

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Table 4-7. Protection table

V_{CC}	V_{BS}	V_{SC}	V_{FO}
< U_{VCC}	X	X	0
15V	< U_{VBS}	0	0
15V	15V	0	H imp
15V	15V	> V_{trip}	0

Note A shoot-through prevention logic prevents $L_{O1,2,3}$ and $H_{O1,2,3}$ for each channel from turning on simultaneously.
Note U_{VCC} is not latched, when Vcc U_{VCC}, FO returns to high impedance.
Note Over-current protection are latched protection and V_{FO} will turn high impedance after the fault condition recovery.

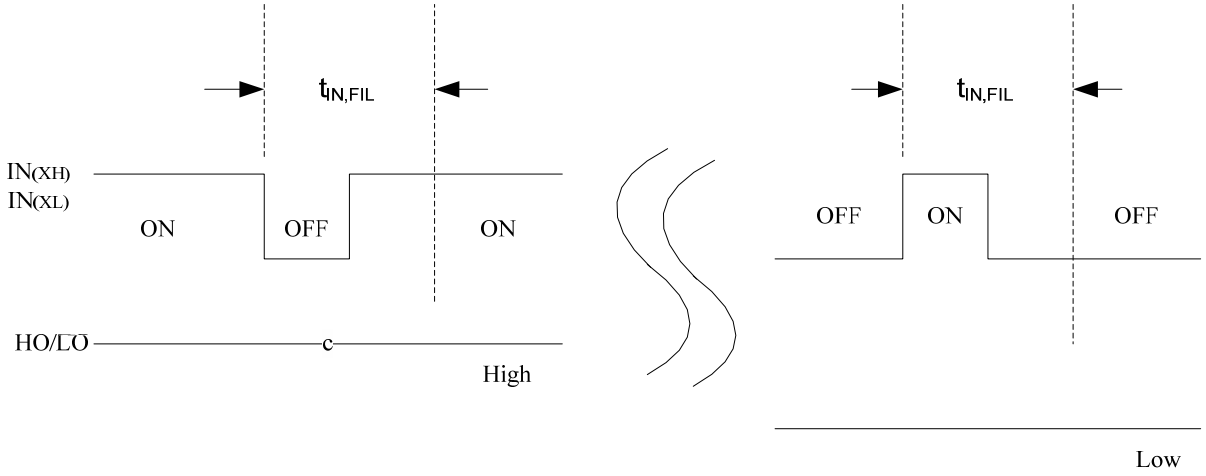


Figure 4-21. Input Filter Function

Note For high side PWM, $IN_{(XH)}$ pulse width must be 1 μ sec.

Reference impedance for trouble shooting

Chapter 5 Safe Operating Area

5.1 Safe operating area of the IPM

5.1.1 Definition of SOA

By built-in gate drive, under-voltage lockout and short-circuit protection guard them from many of the operating modes that would violate the Safe Operation Area (SOA) of the IGBTs in IPM. A conventional SOA definition that characterizes all possible combinations of voltage, current, and time that would cause power device failure is not required. In order to define the SOA for IPM, the power device capability and control circuit operation must both be considered. The resulting easy to apply switching and short-circuit SOA definitions for the IPM is summarized in this section.

The following describes the SOA (Safety Operating Area) of the IPM.

V_{CES} Maximum rating of IGBT collector-emitter voltage

V_{PN} Supply voltage applied on P-N terminals

V_{PN}(surge) The add of V_{PN}

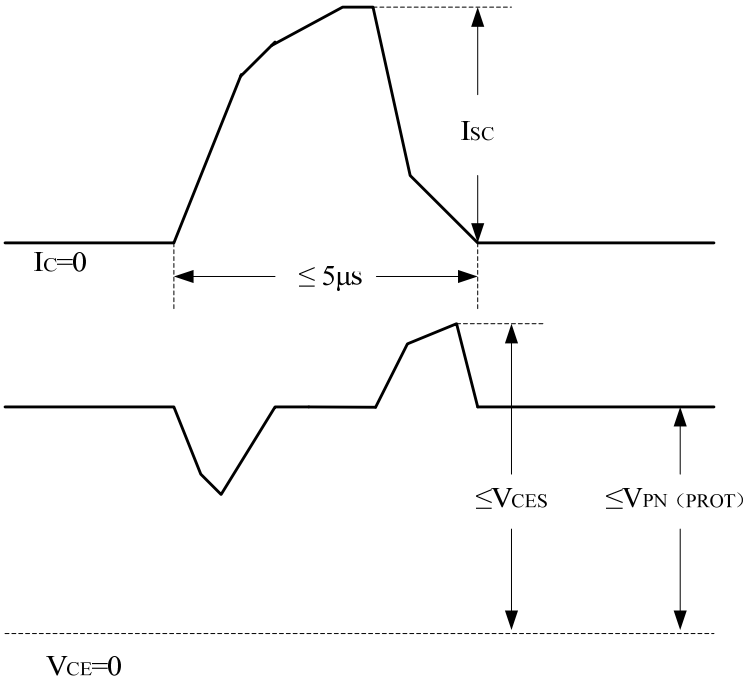


Figure 5-2. SOA for Short-circuit

5.1.2 Switching Operation

In fact, the V_{CES} represents the 600V voltage rating of the IGBTs incorporated into the IPM. But subtracting the surge voltage generated by the stray inductance of the PCB trace and the internal wire bonding of the IPM. Moreover, subtracting from V_{PN}(Surge) the surge voltage generated by the stray inductance between the IPM and the DC-link capacitor is V_{PN} (Surge), please refer to the data sheet for the rated surge voltage .

1. FBSOA – Turn on transition (Power dissipation limited)
2. RBSOA – Turn off transition (Latch-up spec)

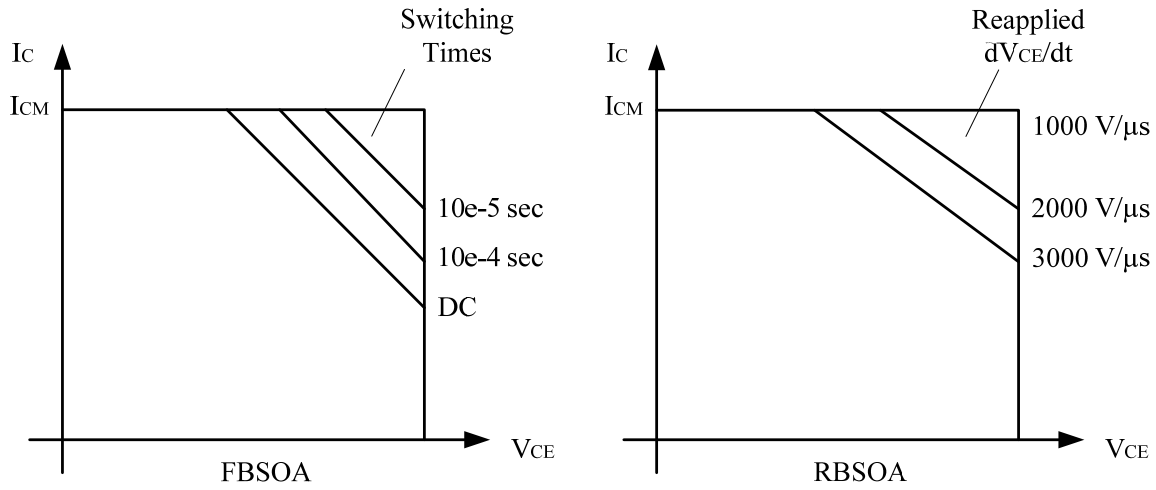


Figure 5-3. Safe Operating Area During Switching

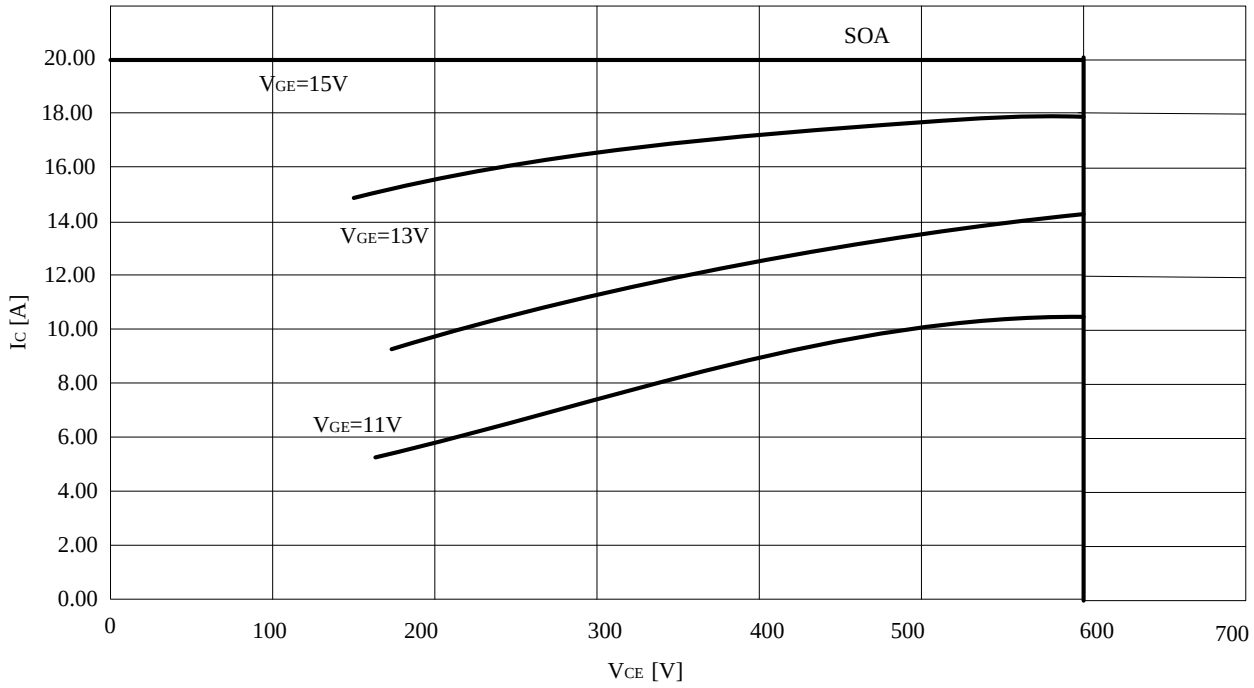


Figure 5-4. Safe Operating Area During Short-Circuit (SCSOA)

V_{CES} represents the 600V voltage rating of the IGBTs incorporated into the IPM. Subtracting the surge voltage (100V or less), generated by stray inductance inside the IPM, from V_{CES} is V_{PN}(Surge), that is, 500V. Moreover, subtracting from V_{PN} (Surge) the surge voltage (100V or less) generated by the stray inductance between the IPM and the DC-link capacitor is $V_{PN(PROT)}$, that is 400V.

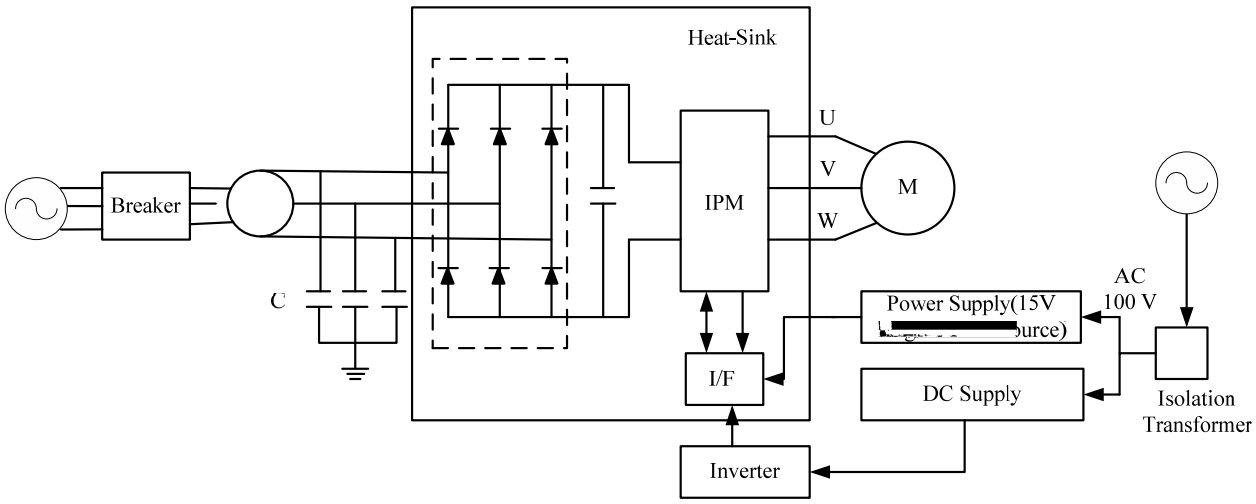
Table 5-1. The Absolute Maximum Rating of P-N Voltage

Items	Symbol	Condition	Rating	Unit
Supply Voltage	V_{PN}	Applied to P-N	450	V
Supply Voltage (Surge)	$V_{PN\ (Surge)}$	Applied between P-N	500	
Collector - Emitter Voltage	V_{CES}		600	
Self protection Supply Voltage Limit (Short-circuit Protective Capability)	$V_{PN(PROT)}$	Applied to DC link, Tj = 125 , Vcc = V_{BS} = 11.5V ~ 20.0V, Non-Repetitive, less than 5us	400	

Note It is recommended that the average junction temperature should be limited to Tj 150 ° C (@ TC ≤ 100 ° C) in order to guarantee safe operation.

5.2 Noise Immunity Capability

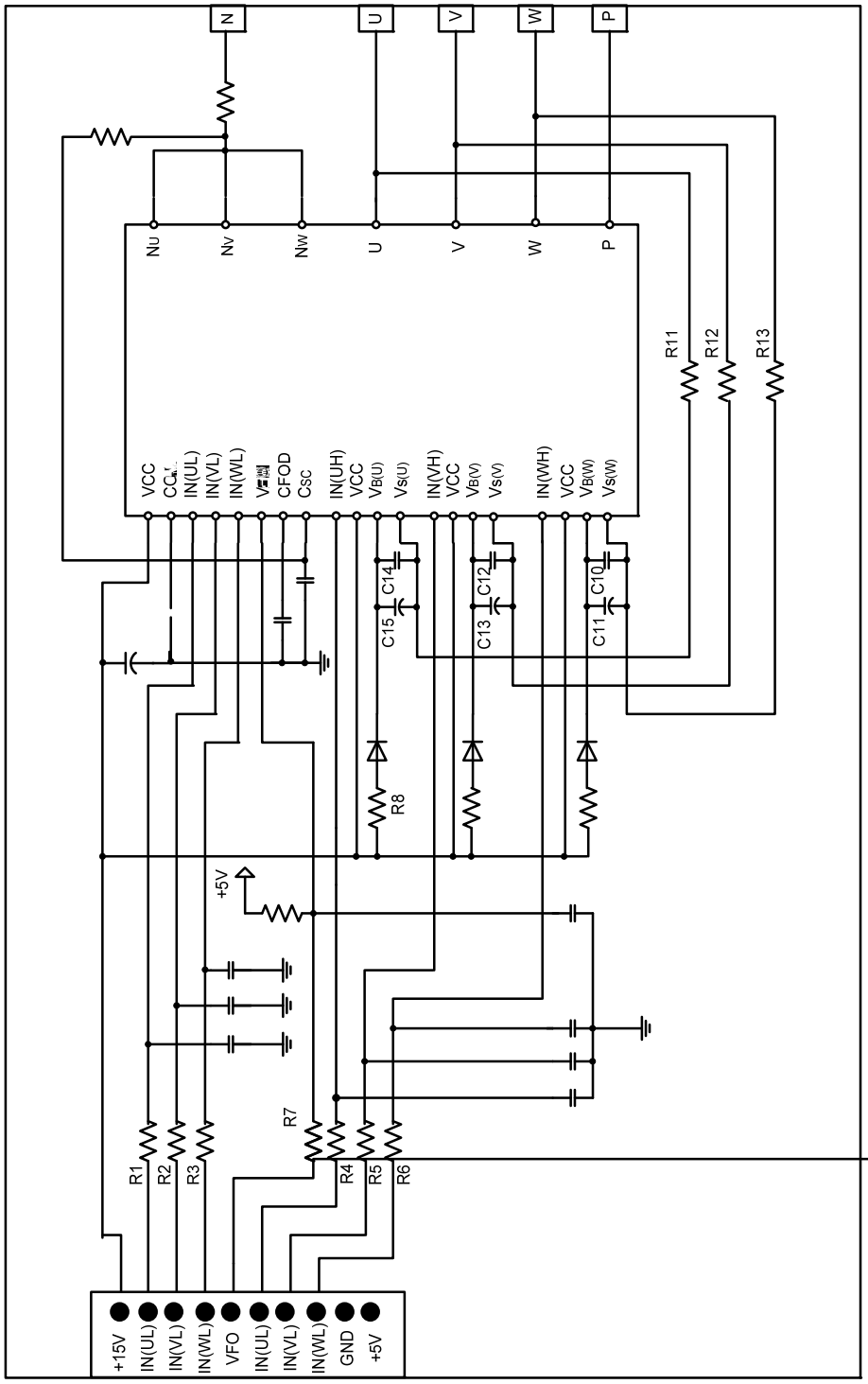
Figure 5-5 shows noise immunity capability testing circuit, ID-IPM have been confirmed to be with ± 2KV noise immunity capability, Noise immunity capability extremely depend on the testing system environment , component layout, control substrate patterns, and other factor, so an additional confirmation on prototype is necessary .


Heat-Sink
U
V
W
M
IPM
Breaker
C
Power Supply(15V
urce)
AC
100 V
I/F
DC Supply
Isolation
Transformer
Inverter

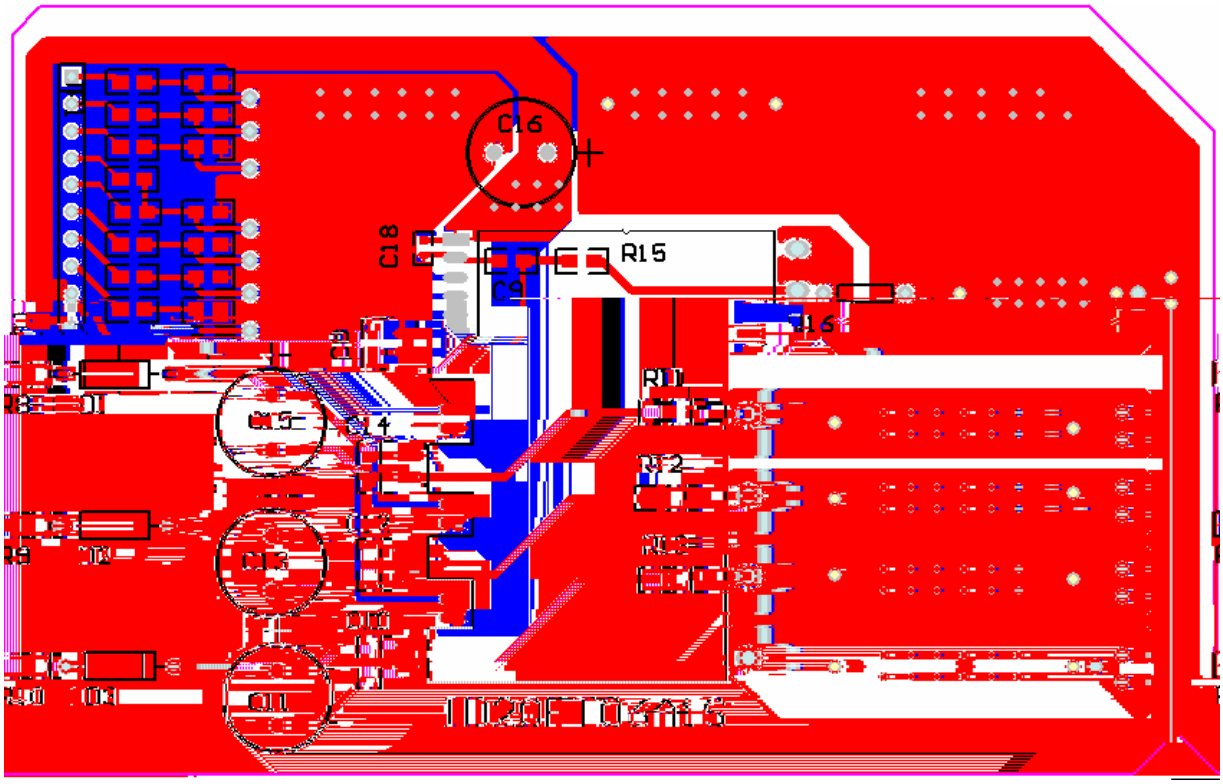
Chapter 6 Reference Design

6.1 Demo board introduction

¸ Demo board schematic



Demo board layout





35	R16	20mΩ 5 W	Non-inductive Resistor	Shunt Resistor for Current Sensing
36	D1	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase U)
47	D2	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase V)
48	D3	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase W)

6.2 Layout Guide-line

- It is recommended that the wiring of the DC- link power path be as short as possible.
- To suppress surge voltage, a non-inductive snubber capacitor should be mounted as close to P and GND (shunt resistor's return pins) as possible.
- The wiring of N terminal and shunt resistors should be as short as possible and shunt resistors' pin connected DC-link GND also should be as short as possible.
- To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible.
- To minimize the pattern impedance, it is recommended that the bootstrap current path be as short as possible.
- FO output is open collector type. The signal line should be pulled up the positive side of the 5V power supply with approximately 4.7kΩ resistance.
- FO output pulse width should be decided by connecting an external capacitor between CFO and GND terminals.
- Each input signal line should be pulled up to the 5V power supply with approximately 680Ω~4.7kΩ resistance. Approximately a 0.22~2μF by-pass capacitor should be used across each power supply connection terminals.
- In order to provide good decoupling between Vcc-GND and V_B-V_S terminals, the capacitors shown connected between these terminals should be located very close to the module pins. AddiGesAddirquescyca



Chapter 7 Thermal Resistances Concepts Introduction

7.1 Overview

Semiconductor devices are very sensitive to junction temperature, i.e., as the junction temperature increases, the operating characteristics of a device are altered from normal, and the failure rate increases exponentially. This makes the thermal design of the package a very important factor in the device development stage, and also in an application field.

To gain insight into the device's thermal performance, it is normal to introduce thermal resistance. The thermal resistance is a measure of the temperature change across a package caused by power dissipation of the packaged semiconductor device. It is an indication of the heat transfer from the semiconductor device through the package materials out to the environment in terms of temperature per unit of power. Thermal resistance data can be used by the de-signer or customer to estimate the junction temperature of their die in operation.

Figure 7-1 shows a thermal network of heat flow from junction-to-ambient for the SDIP-IPM including a heat sink.

The thermal resistance of the ID-IPM is defined in the following equation.

The thermal resistance of a semiconductor device is generally as

$$R_{\theta JX} = \frac{T_J - T_X}{P_H} \tag{7-1}$$

Where $R_{\theta JX}$ = Thermal resistance from device junction to the specific environment (alternative symbol is θ_{JX}) [/W]

T_J = device junction temperature in the steady state test condition [ ]

T_X = reference temperature for the specific environment [ ]

P_H = power dissipated in the device [W]

The selection of a reference point is arbitrary, but usually the hottest spot on the back of a device on which heat sink is attached is chosen. This is called junction-to-case thermal resistance, $R_{\theta JC}$.

$$R_{\theta JC} = \frac{T_J - T_C}{P_H} \tag{7-2}$$

Where T_C = device case temperature in the steady state test condition [ ]

When the reference point is an ambient temperature, this is called junction-to-ambient thermal resistance, $R_{\theta JA}$.

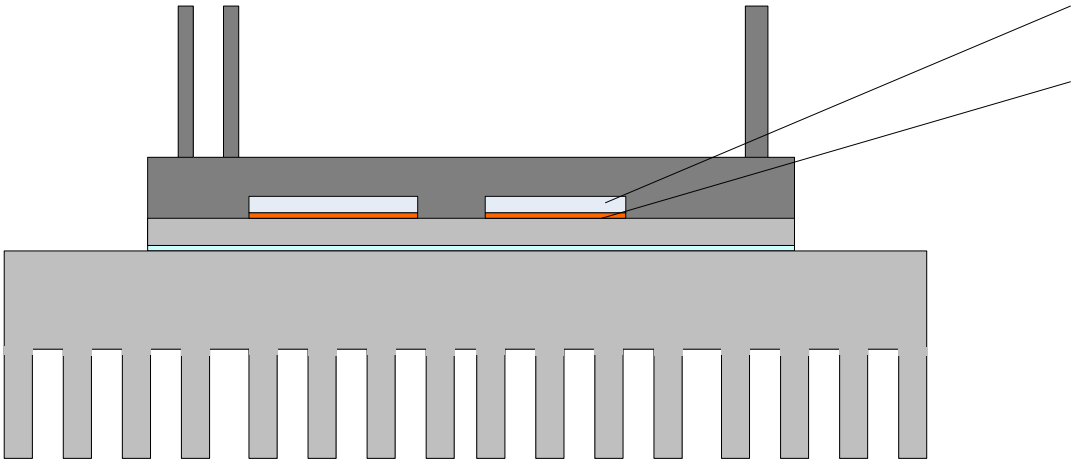
$$R_{\theta JA} = \frac{T_J - T_A}{P_H} \tag{7-3}$$

Where T_A = Ambient temperature [ ]

$R_{\theta JA}$ (/W) indicates the total thermal performance of the SDIP-IPM including the heat sink. Basically $R_{\theta JA}$ is a serial summation of various thermal resistances, $R_{\theta JC}$, $R_{\theta CG}$, $R_{\theta GH}$ and $R_{\theta HA}$.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CG} + R_{\theta GH} + R_{\theta HA} \quad (7\text{-}4)$$

Where, $R_{\theta CG}$ is contact thermal resistance due to the thermal grease between the package and the heat sink, and $R_{\theta GH}$ is heat sink thermal resistance, respectively. From the equation (7-4), it is clear that minimizing $R_{\theta CH}$ and $R_{\theta HA}$ is an essential application factor to maximize the power carrying ability of the device as well as the minimizing of $R_{\theta JC}$ itself. Usually the value of $R_{\theta CH}$ is proportional to the thermal grease and governed by the skill at the assembly site, while $R_{\theta HA}$ can be handled to some extent by selecting an appropriate heat sink.



The Electrical Test Method (ETM) uses the forward voltage dropped of a junction as the temperature sensitive parameter and is variously known as the “diode-forward-drop” method from original applications with power diodes and bipolar power transistors. It is based on a temperature and voltage dependency exhibited by all semiconductor diode junctions. This relationship can be measured and used to compute the semiconductor junction temperatures in response to power dissipation in the junction region. The voltage-temperature relationships are an intrinsic electro-thermal property of semiconductor junctions, and are characterized by a nearly linear relationship between forward-biased voltage drop and junction temperature when a constant forward-biased current is applied. This constant current is called the “sense current” (also “measurement current”). This voltage drop of the junction is called Temperature sensitive Parameter (TSP). Figure 7-2 illustrates the concept of measuring this voltage versus junction temperature relationship in for a diode junction. The device under test (DUT) is embedded in hot fluid to heat DUT up to desired temperatures.

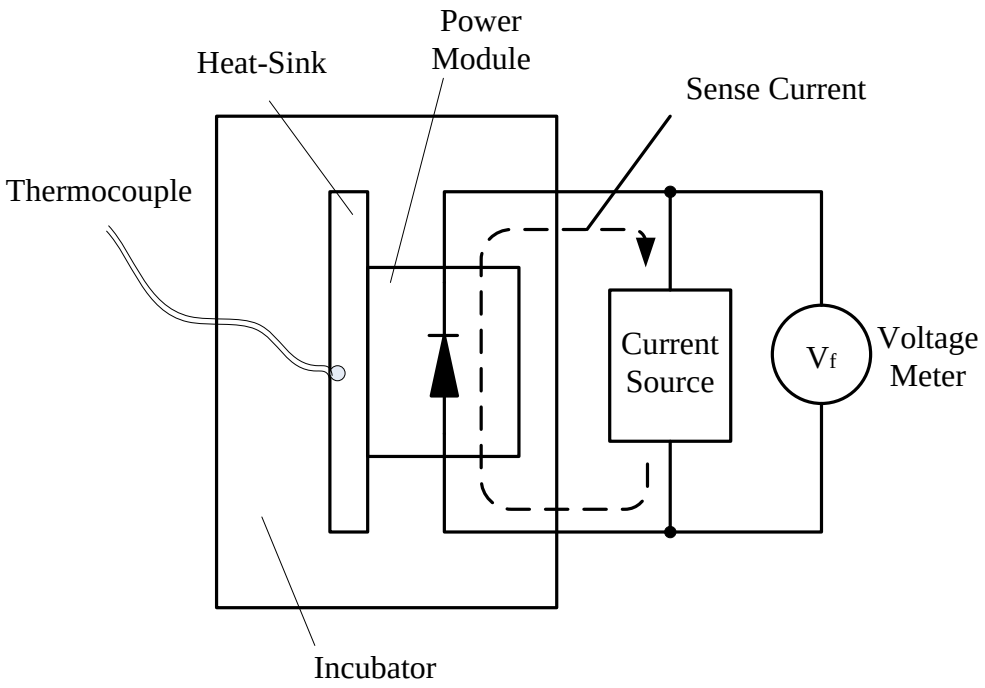


Fig. 7-2 Illustrations of the Bath Method for TSP Measurement

When the DUT attains thermal equilibrium with the hot fluid, a sense current is applied to the junction. Then the voltage drop across the junction is measured as a function of the junction temperatures. The measurement current through the temperature sensing diode must be large enough to obtain a reliable forward voltage reading not influenced by surface leakage effects but small enough not to cause significant self heating. For instance, 1mA, 10mA depending on the device type. The measurements are repeated over a specific temperature range with some specified temperature steps. Figure 7-3 shows a graph of typical result.



calibrating parameters.

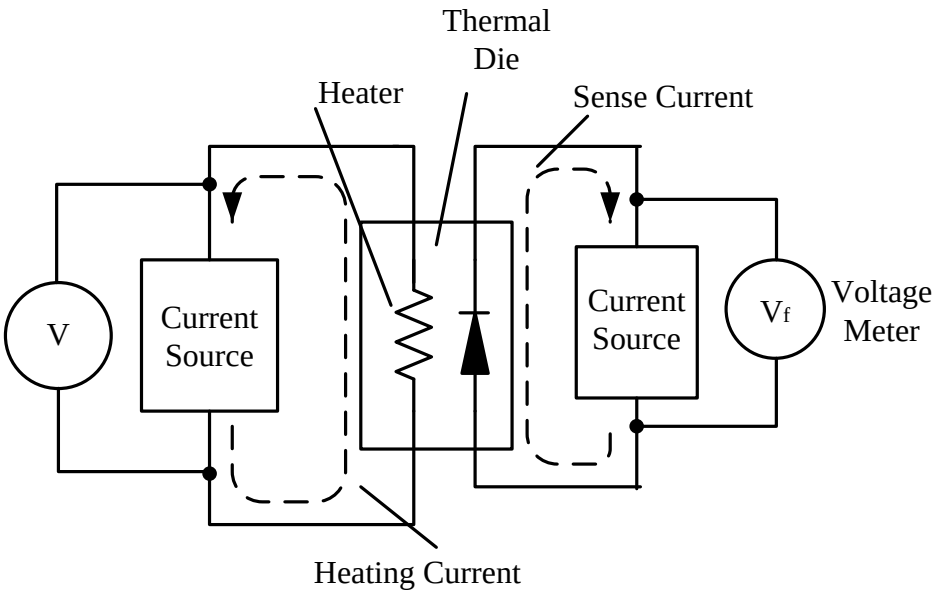
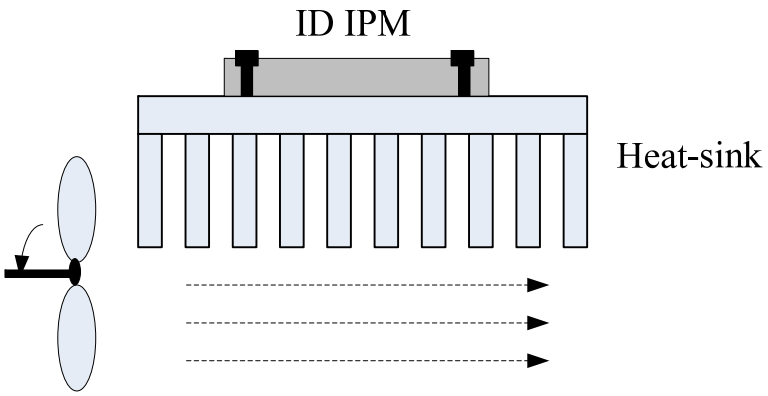


Fig. 7-4 Illustration of Thermal Test Die Test Method Concept

Active Dice

Active or functional dice are often used as the ultimate test for component thermal characterization. The primary feature that distinguishes active die from thermal die is that heat dissipation is not electrically independent from temperature sensing and that the die is designed to perform an electrical function than providing convenient junction temperature reporting. This requires that the otherwise continuous heating power be interrupted for the measurement of the junction temperature. The process of periodically interrupting the heating power to measure the sense junction voltage is best presented with some standard definitions.

The thermal resistance test begins by applying a continuous power of known voltage to the DUT. The continuous power heats up the DUT to a thermal equipment state. The heating interval is the period of time when the heating power is being delivered to the component under test. Active dice are tested with a succession of heating intervals and temperature sampling intervals. During thermal resistance testing, the heating intervals are much longer than the temperature sampling intervals; the heating duty-cycle approaches 100%, which for all practical purposes is considered to be continuous power. Temperature sampling interval is the period of time when the heating power has been interrupted and the sense current has been applied to the sensed junction. The temperature sensitive voltage is measured during this interval. It must be very short so as not to allow for any appreciable cooling of the junction prior to re-applying power. Figure 7-5 illustrates the heating and measurement intervals.


ID IPM
Heat-sink

Prerequisites:

For approximate power loss calculations, the following prerequisites are necessary

1. Sine waveform current output PWM control VVVF inverter

8.2 Switching Loss and Calculation Method

Switching loss can be calculated form turn on/off time and over-voltage / current characteristics.
In high frequency PWM switching losses can be extensive and must be considered in thermal design.
The most common method of determining switching losses is to plot the IC and Vce waveforms during the switching transition .Figure 8-3 shown is typical of hard switched inductive load application ex. motor driving application.

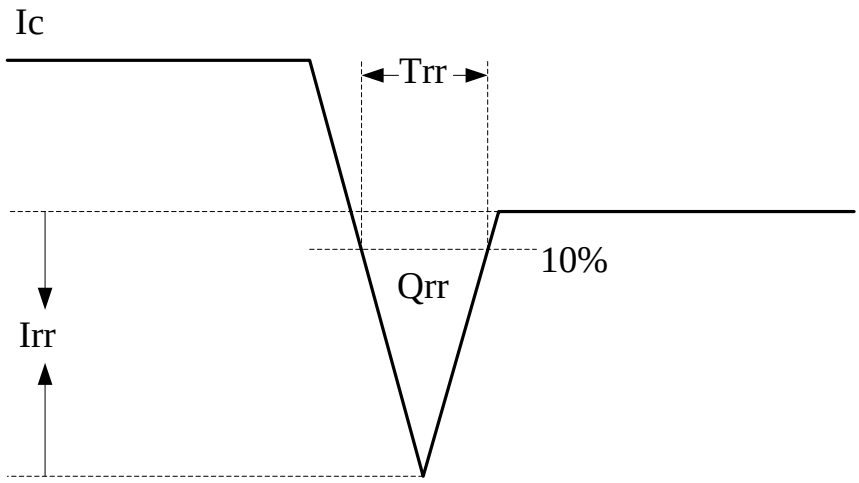


Figure 8-3 Diode loss

Therefore, the loss of diode is idealized as shown in Figure 8-3 and recovery occurs in the middle of output current period. Therefore the formula is below:

$$P_{SW(Diode)} = \frac{1}{2} \times f_c \times \frac{I_{rr} \times t_{rr} \times V_D}{4}$$

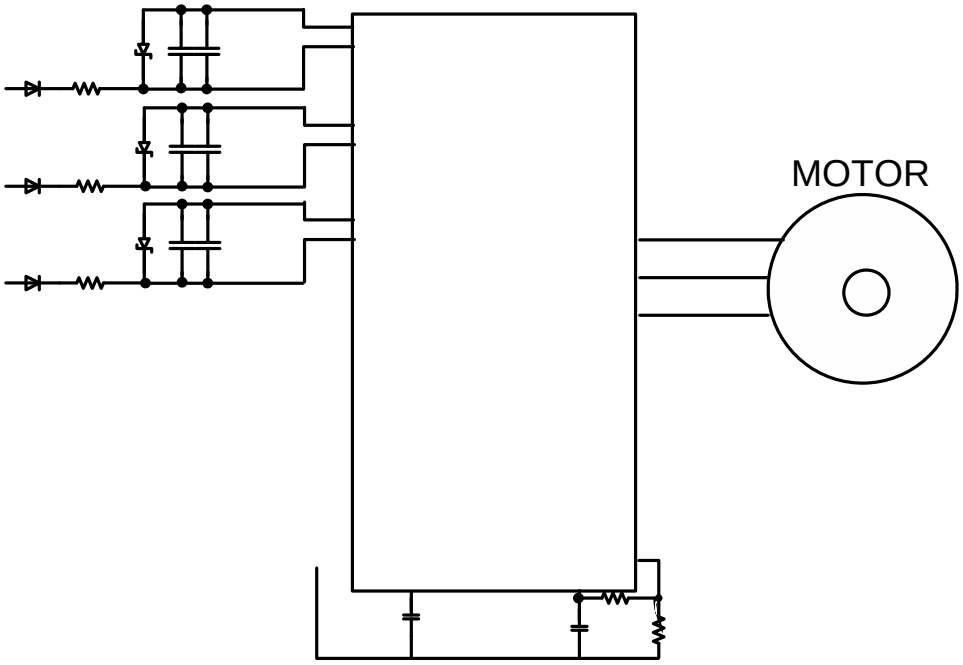
IGBT power loss = $P_{IGBT} + P_{SW(IGBT)}$

Diode power loss = $P_{Diode} + P_{SW(Diode)}$

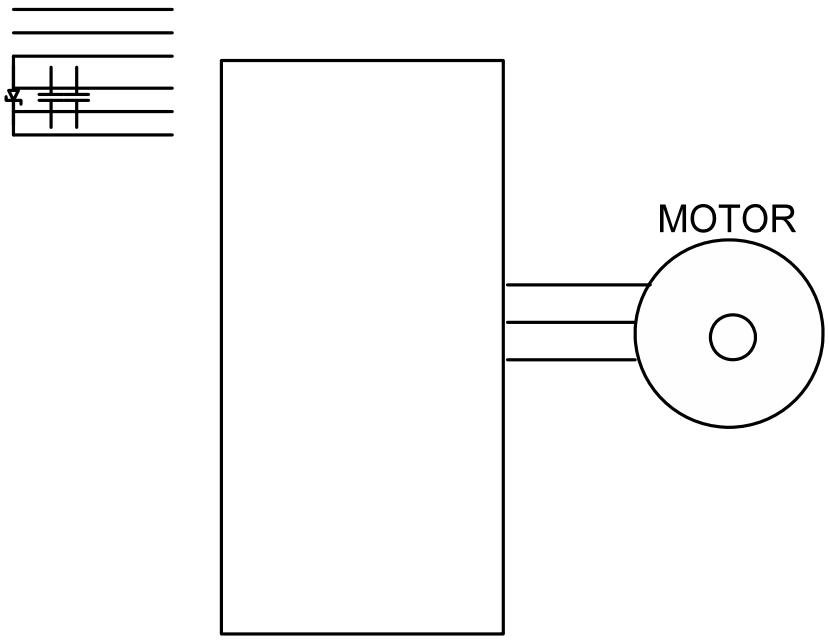
Chapter 9 Appendix Document

9.1 F.A.Q for Starpower ID IPM

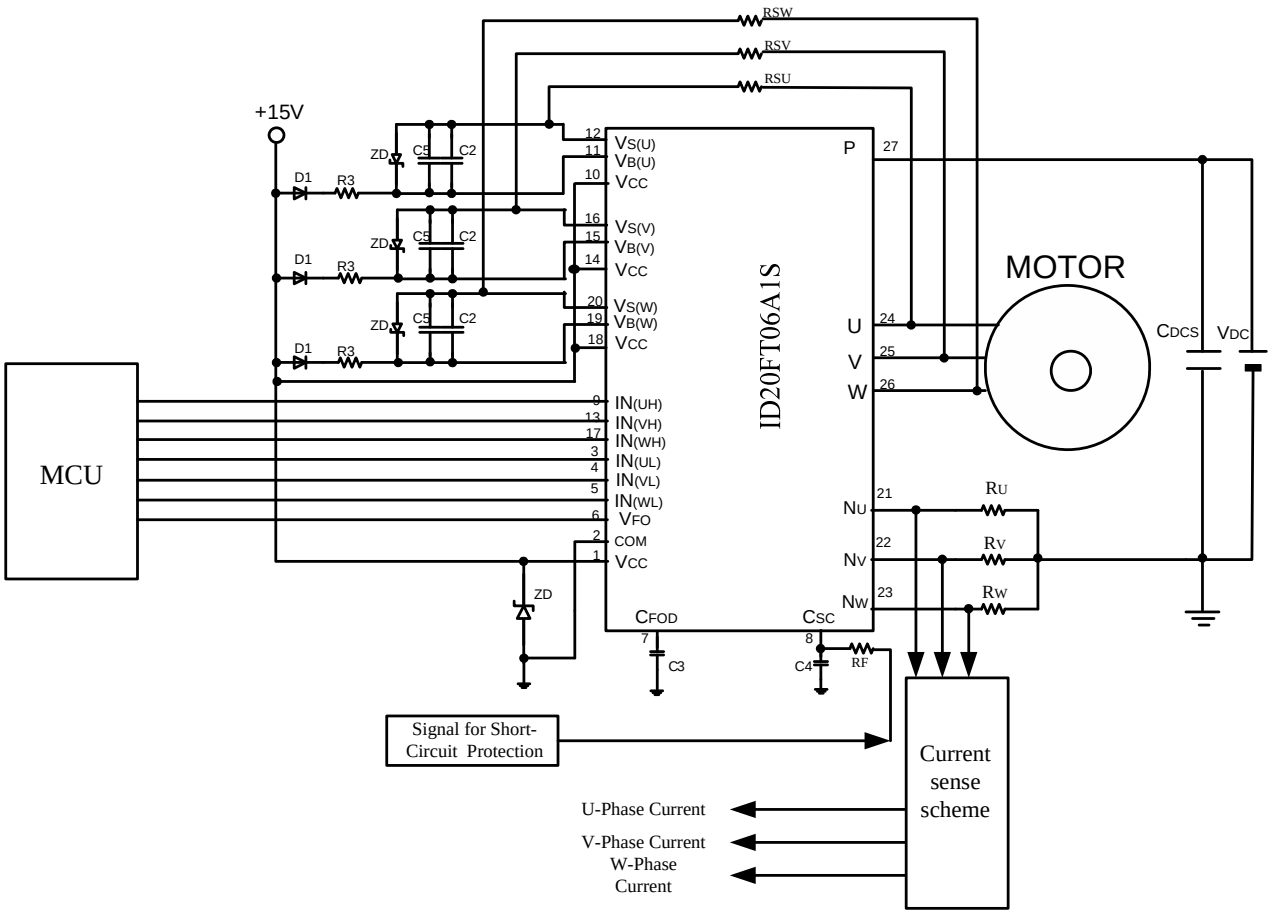
1) Circuitry reference design for application



2) Can not start up the system after adopt IPM, or system shut-off immediately after start up.



9.2 Divided negative dc-link terminals for current sensing applications



IPM selection reference

Part Number	IGBT Ratings	General Applications		Remark
		PWM Frequency(Typ.)	Motor Ratings(*)	
ID10FT06A1-S	600V/10A	15kHz	0.5 KW/220Vac	V_{iso} = AC 2500V_{rms} (Sinusoidal 1min)
ID15FT06A1-S	600V/15A	15kHz	0.75 KW/220Vac	
ID20FT06A1-S	600V/20A	15kHz	1.5 KW/220Vac	
ID30FT06A1-S	600V/30A	15kHz	2.2 KW/220Vac	